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# NAVAL POSTGRADUATE SCHOOL

## Monterey, California

DATA ACQUISITION UNIT FOR

SATCOM SIGNAL ANALYZER

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Project Report

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A Data Acquisition Unit has been designed, constructed and demonstrated as part of the SATCOM SIGNAL ANALYZER. This unit converts Intermediate Frequency analog UHF satellite signals to digital data, stores the digital data in buffer memory, and interfaces with a host computer to facilitate passing the digital data to the host computer.

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## TABLE OF CONTENTS

## LIST OF FIGURES

<u>LIST OF TABLES</u>

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# I. INTRODUCTION

## A. BACKGROUND

This project is part of a series of research projects undertaken by the NAVPGSCOL Satellite Communications Laboratory concerning Navy UHF Satellite Communications. In March of 1977, this Laboratory received funding from PME 1Ø6-1 of NAVELEX to develop, design and construct a SATCOM Signal Analyzer at NAVPGSCOL. The purpose of the SATCOM Signal Analyzer is to provide high-speed spectrum analysis of the Navy UHF communication satellite transponders while in orbit.

## B. SPECIFIC GOALS

The specific goals in the development of this system are (1) to provide all necessary equipment to make real-time measurements at the Naval Postgraduate School; (2) to develop satellite signal analysis techniques; and (3) to provide equipment design for use in a follow-on version of the Fleet Satellite Monitoring System (FSM) presently in use at the Naval Communication Stations to monitor GAPFILLER and FLTSAT satellites.

## C. SCOPE OF THIS REPORT

Figure 1 is a simplified block diagram of the Satellite Signal Analyzer System. This report documents the design and construction of the Data Acquisition Unit, plus the first phase of spectrum analysis software. Additionally, this re-

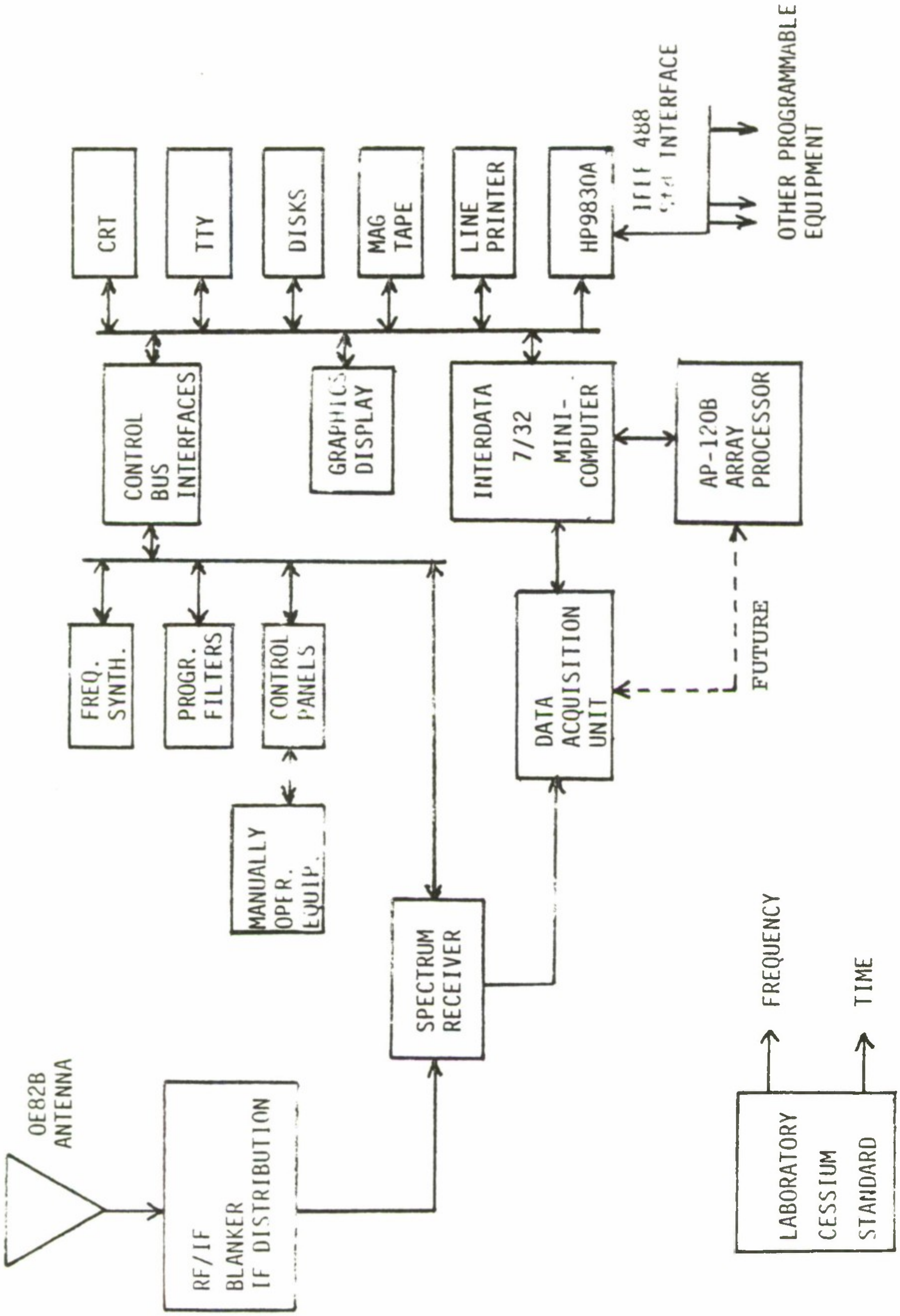



Figure 1. Signal Analyzer System Simplified Block Diagram.

port deals with theoretical implications related to the practical application of dual channel A/D conversion of signal data.

D. SATELLITE SIGNAL ANALYZER

The Satellite Signal Analyzer has been constructed around an INTERDATA 7/32 minicomputer system, which provides all the necessary control for most of the equipment in the system. High speed processing has been provided via the Floating Point Systems AP-120B Array Processor as a peripheral device to the INTERDATA 7/32. Additional standard peripherals are provided for display, control and software support functions as shown in Figure 1.

The Spectrum Analyzer has been implemented using digital techniques which overcome many of the shortcomings of the present FSM. Dual channel, inphase and quadrature, down conversion of the signal is used to produce two baseband signals which are simultaneously sampled, held and analog-to-digital converted to form the "real" and "imaginary" components of a complex waveform. As explained in Reference 1 this technique preserves all of the band pass characteristics of the RF as shown below, and illustrated in Figure 2.

Local oscillator signal: $\cos(\omega_L t)$

RF (or IF) signal: $x(t)$

"IN-phase" component: $I(t) = \cos(\omega_L t)x(t)$

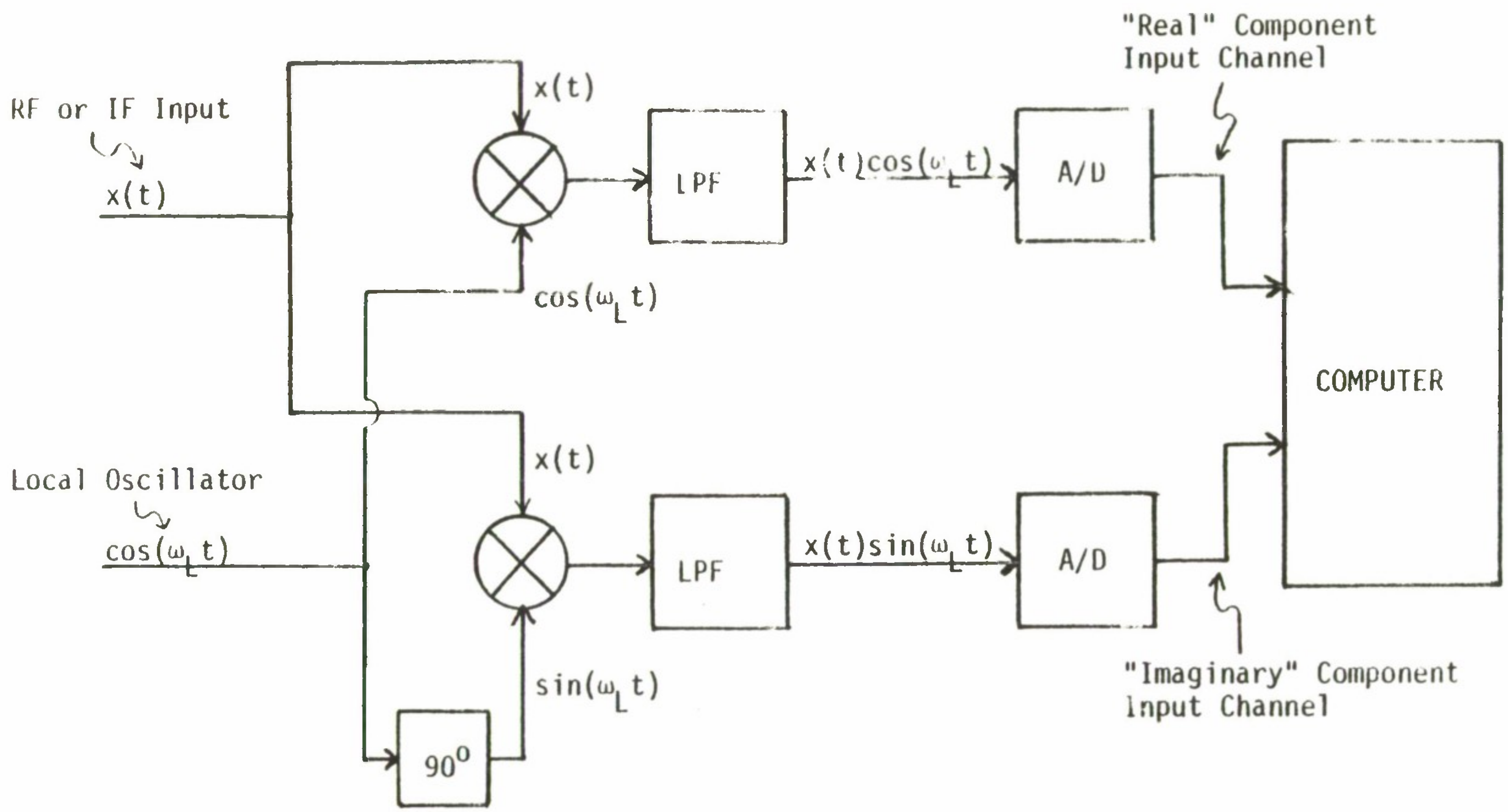



Figure 2. Dual Channel Down-Conversion Technique.

"Quadrature-phase" component: $Q(t) = \sin(\omega_L t)x(t)$ combining as "real" and "imaginary" components of a "complex" signal:

$$
\begin{aligned}
y(t) &= I(t) + jQ(t) \\
&= \cos(\omega_L t)x(t) + j\sin(\omega_L t)x(t) \\
&= \left[\cos(\omega_L t) + j\sin(\omega_L t)\right] x(t) \\
&= e^{j\omega_L t}x(t)
\end{aligned}
$$

and taking the Fourier Transform,

$$
\begin{aligned}
F\{y(t)\} &= F\{e^{j\omega_L t}x(t)\} \\
&= F_x(\omega - \omega_L)
\end{aligned}
$$

Thus, the D.C. component in the baseband signal is the component in the RF signal at the frequency of the local oscillator. This technique permits digital sampling at baseband frequencies while retaining all passband information. Digital spectrum analysis provides a spectral presentation which has no time ambiguity, i.e., all frequency components existed throughout the sampling period. The present FSM uses an analog spectrum analyzer with a scanning display (driven by a computer) so that each frequency component is sampled at a different time with possible several seconds between start and completion of scan. This method can produce very misleading presentations, particularly when using Time Division

Multiple Access techniques in SATCOM channel assignments with access time measured in seconds.

E. DATA ACQUISITION UNIT

The Data Acquisition Unit, DAU, is that portion of the SATCOM Signal Analyzer that converts intermediate frequency, IF, analog UHF satellite signal to digital signal data. The DAU also stores the converted data in buffer memory and then interfaces with the INTERDATA 7/32 minicomputer in order to pass the data on for signal processing.

Reference 1 specified that the DAU be capable of providing the following capability:

1. Dual channel simultaneous sample and hold at clock rate up to 3 MHz.

2. Analog-to-digital convert both channels in parallel with 8 bit resolution at 3 MHz, and 12 bit resolution to 400 KHz.

3. Perform all conversion under computer control.

4. Store data as necessary for DMA (Direct Memory Access) input to computer or array processor. If direct input is not possible at highest rate, store at least 2048 data values for each channel.

5. Provide expansion capability for additional pairs of sample/hold and A/D converters.

After a search of the literature on data acquisition systems failed to reveal an appropriate commercially available unit capable of meeting the stated requirements, the task of building a Data Acquisition Unit was undertaken in this laboratory.

## II. DATA ACQUISITION UNIT

### A. GENERAL INFORMATION

#### 1. Introduction

The task of designing and constructing a Data Acquisition Unit that could perform as specified, was undertaken by this laboratory in order to fulfill the larger requirement of building a SATCOM Signal Analyzer. The Data Acquisition Unit had to be capable of: 1) Dual channel sample and hold to 3 MHz sample rate; 2) Analog-to digital conversion of two channels in parallel with 8 bit resolution at 3 MHz sample rate and 12 bit resolution to 4ØØ KHz; 3) Performance by computer control; 4) Provision for buffer memory data storage; 5) Provision for expansion.

#### 2. Theory of Dual Channel Analog-to-Digital Conversion

Nyquist sample-rate theory requires that at least two samples per cycle, for the highest frequency in the signal, be taken in order to recover all of the signal information. For a baseband signal, using a single A/D converter, the sample rate would be at least twice the frequency of the highest frequency component in the signal. By using dual channel A/D conversion certain advantages become available.

As described in Sec I.C.1.b. an RF or IF signal can be reconstructed at baseband from the "Inphase" and "Quadrature" downconverted signal components. This method gives two distinct baseband signals, 9Ø degrees out of phase with each other, derived from the same source. By sampling and A/D converting both baseband signals simultaneously, numerical estimates of the instantaneous inphase and quadrature signal components are obtained. This inphase and quadrature numerical pair can then be used to represent the real and imaginary components of a complex data point. Utilizing two A/D converted numbers as one complex data point allows that each A/D converter need only operate at a sample rate at least as high as the highest signal frequency component vice at twice the frequency. Additionally, the complex data points, when processed with the Fast Fourier Transform (FFT), permits a more efficient use of the algorithm, whereby all of the computed results are meaningful. The single channel (real component only) FFT produces a symmetric output, half of which is redundant. This dual channel technique retains all of the passband information of the original IF or RF signal, where the zero frequency component corresponds to the component of the RF signal at the local oscillator frequency.

Thus by using dual channel A/D conversion, either twice as wide a signal bandwidth can be analyzed or alternately A/D converters with only half the speed performance need be used. Also the FFT algorithm is used efficiently, completely reconstructing the RF signal passband around the zero frequency component in the FFT output.

For clarification, the remainder of this thesis will refer to the inphase signal component as channel one data and the quadrature signal component as channel two data.

3. Sample Rate Requirements

Assuming that sampling will be done at frequencies greater than the Nyquist rate, what should be the practical upper limit of the sampling frequency? The Nyquist rate requirement applies to any signal component within the signal bandwidth regardless of the signal level. Because no filter can provide a perfect rectangular passband, the upper frequency cutoff must be determined in order to produce digital signal processing with minimum aliasing.

The widest filter bandwidth in the SATCOM Signal Analyzer is 1 MHz for the spectrum receiver, A25, with a fourth order roll off. A high speed A/D conversion time of 200 nanoseconds was specified for the DAU. This assured a 4 MHz sample rate upper limit which allows sampling at twice the Nyquist rate of 2 MHz for the 1 MHz bandwidth. For a fourth order filter the signal components fall off at 24 dB per octave which means at 4 MHz all signal components will be down 4Ø dB, a satisfactory level for this application.

4. Bit Resolution Requirements

For the GAPFILLER wideband channel spectrum requirements, it was considered adequate to use an analog-to-digital conversion signal-to-noise (SNR) of approximately 49 dB. When considering how may bits of analog-to-digital conversion (ADC) resolution are required, the ADC quantization noise contribution must be considered. A good engineering "rule of thumb" is that A/D converters provide 6 dB of signal to quantization noise per bit of resolution. Hence, an eight bit ADC would provide 48 dB of signal to noise ratio against a full scale signal. For the high speed A/D converters designed primarily to provide spectral information for the wideband channel, eight bit resolution was chosen as adequate. Using 12 bit ADC resolution provides 72 dB SNR which would add negligible noise level to any signal and provides increased dynamic range. Thus the low speed A/D converters have 12 bit resolution and will provide signal conversion to sample rates to 400 Kilohertz.

## B. GENERAL DESCRIPTION

### 1. Introduction

Figure 3 is a block diagram of the Data Acquisition System. This system has been designed with signal input ports for two channels of IF input and two Local Oscillator (LO) inputs for inphase and quadrature downconversion to baseband. Additionally, signal input ports for two channels of external baseband signals have been provided through the front panel. The Data Acquisition Unit contains an integral frequency synthesizer for sample rate control, two dual-channel A/D converter units, a dual channel buffer memory unit, and a parallel data interface to the INTERDATA 7/32. Sample rate, word count, start address in buffer memory, A/D converter selection, start acquisition and reset are

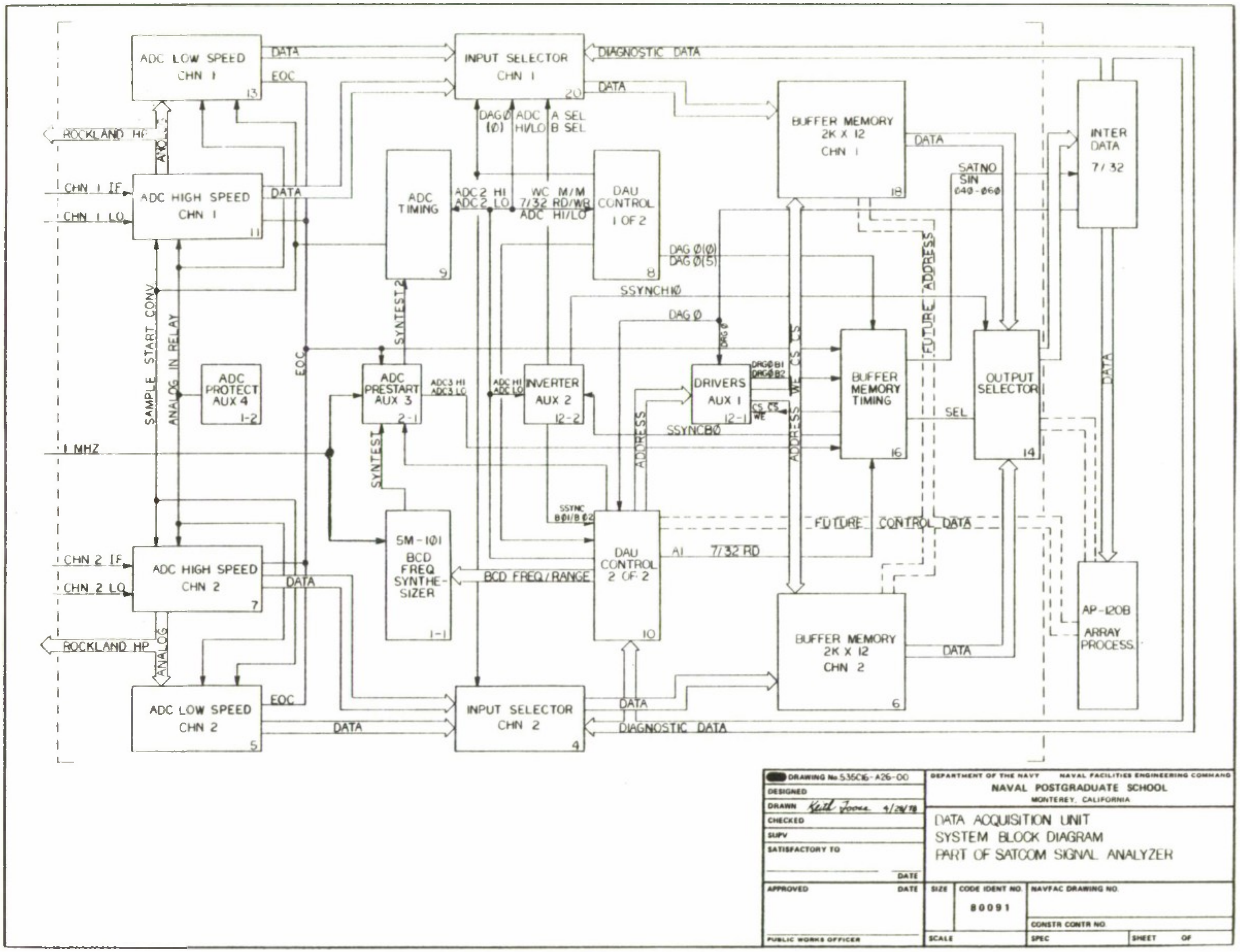



Figure 3 - Data Acquisition Unit Block Diagram

under control of the INTERDATA 7/32. Data transfer, presently only to the INTERDATA 7/32, will ultimately be made directly to the Floating Point Systems AP-12ØB Array Processor. The AP-12ØB I/O port, IOP-16, will ultimately control the data transfer from the DAU to the AP-12ØB. However, the AP-12ØB will remain under control of the INTERDATA 7/32.

2. Analog-to-Digital Converter Unit

a. High Speed ADC Boards

The DAU contains two printed circuit boards, one each for channel 1 and channel 2, to provide for high speed A/D conversion. Additionally the High Speed ADC boards provide, 1) IF to baseband downconversion, 2) External to IF switching, 3) Baseband signal amplification, 4) Buffered signal to HP-122Ø oscilloscope and Rockland filter (eventually to Low Speed ADC boards). The sample-and-hold modules used are DATEL Systems model SHM-UH 2ØØ picosecond aperture time units. Paired with the SHM modules are DATEL Systems model ADC-VH8B2 8 bit, 2ØØ nanosecond, A/D converter modules. The A/D converters provide parallel output which is latched on the ADC boards for stability and buffering in the DAU. The High Speed boards are used for sample rates to 4 MHz.

b. Low Speed ADC Boards

Two printed circuit boards, one each for channel 1 and channel 2, are dedicated to low speed A/D converter units. The sample-and-hold function is provided by DATEL

Systems, model ADC-EH12B3 12 bit, 2.Ø microsecond A/D converter modules are used to provide parallel output to on board latches. The Low Speed boards are used for high resolution sample rates to 4ØØ Kilohertz.

3. Sample Rate Frequency Synthesizer

Sample Rate is provided by a SYNTEST-SM1Ø1 frequency synthesizer [Ref. 3] which is Binary Coded Decimal (BCD) programmable with four BCD digits of frequency plus one for range to provide TTL compatible output from .1 Hz to 16 MHz. Programming is provided from RANGE and FREQUENCY registers on the control Interface Board discussed in Section II.C.12. Sample rate may be changed at any time but is software limited to other than data acquisition times. The SM-1Ø1 provides clocking through the ADC Prestart Board to the ADC Timing Board for synchronization of sample command and start convert pulses.

4. Data and Control Input/Output

The Data Acquisition Unit operates under control of the INTERDATA 7/32 via the INTERDATA Universal Logic Interface (ULI), INTERDATA Product M 48-Ø13, [Ref. 2]. The INTERDATA 7/32, ULI provides Input/Output (I/O) for 16 Data Out (DOT) lines, 16 Data In (DIN) lines, four Control Out (COT) lines, eight Status In (SIN) lines, and one each additional lines, Data Available, Gated (DAGØ), Data Request, Gated (DRGØ), Status Attention (SATNØ), and Status Clear (SCLRØ).

Connectors 2 and 3 of the ULI have been rewired to place all signals on 28 gauge twisted pair cable for connection to the DAU. One 7438 NAND driver has been added in the optional component area of the ULI to provide drive for the DAG0 and DRGØ signals.

The above described ULI lines enter the DAU through the DAU backplane to be distributed to the Control Interface Board (1 of 2) and (2 of 2). The DOT lines also parallel to the DAU Input Selector boards and the DIN lines parallel to the DAU Output Selector board to provide data in and data out buses respectively, to and from the DAU.

5. Buffer Memory

As has been shown, the DAU has the capability of generating pairs of digital data words at up to a 4 MHz rate. However, the INTERDATA 7/32 can only Direct Memory Access (DMA) 16 bit words, i.e., transfer data, at a rate slightly less than 1 MHz. Alternately in the future configuration with the DAU transferring data directly to the AP-12ØB, 16 bit word DMA through the IOP-16 is constrained to 1.5 MHz. Clearly then, considering that two 16 bit words must be transferred from the DAU for each pair it acquires, the DAU must store intermediate data in order to acquire data at full sample rate capacity. To be compatible with the dual channel A/D conversion, two channels of buffer memory, designed around FAIRCHILD 93415 1Ø24X1 Bipolar RAM MEMORY I.C.'s, were built into the DAU. Bipolar RAM MEMORY was used despite its higher power consumption to take advantage of its 35 nanosecond access time necessary for the 4 MHz acquisition rate.

This laboratory's AP-120B as configured has the capability of performing the FFT algorithm on data blocks up to a maximum of 2Ø48 complex points. Thus, the DAU buffer memory was designed to contain 2Ø48 pairs of 12 bit words, which allows continuous acquisition of the maximum size FFT block useable in the AP-12ØB. The buffer memory is contained on two boards, one for each channel.

6. Control

To maintain INTERDATA 7/32 control of the DAU, the control interface circuitry is built on two boards named Control (1 of 2) and Control (2 of 2). Control board (1 of 2) is mainly comprised of registers for programming range and frequency of the SM-1Ø1 frequency synthesizer, plus block word count and block starting address, plus a register to control the operational mode of the DAU. Control board (2 of 2) contains error condition sensors and a status register to interface DAU operational conditions to the INTERDATA 7/32 and provide "handshaking" signals.

7, Front Panel

The DAU front panel simply consists of two toggle switches to allow switching the analog signal input for the channel one and channel two A/D converters between the NORMAL spectrum receiver signal or an EXTERNAL supplied signal.

Below the toggle switches, female BNC connectors are provided for connection of the external signal. Finally the front panel has one LED located in the bottom left corner to indicate that all DAU power supplies are operational.

8. Construction

As a prototype the DAU was constructed with ample space both on individual printed circuit boards and in the printed circuit board 19 inch rack mounted housing. The P.C. boards are mounted vertically in two rows from front to back as shown by the top view in Figure 4. The front row of P.C. boards are 9 inches wide by 9 inches high while the back row of P.C. boards are 10 inches wide by 9 inches high. The P.C. boards are supported by vertical card guides and fitted into two 36 pin wire wrap connectors per board. This configuration forms a plane of wire wrap posts on the bottom of the DAU housing for interboard wiring connections. The back of the housing contains three small power supply modules, two protection relays, plus wire strips for additional power supply connections. Additionally the back contains two 50 pin connectors that connect to the INTERDATA 7/32 or the DAU Test Panel as necessary. Adequate room remains on the back plane for future connector installation to support interconnection to the AP-120B's, IOP-106. The back plane connectors are wire wrapped into the bottom plane to distribute signals to and from the DAU. Several specific signal paths were interconnected with 50 ohm coaxial cable to insure

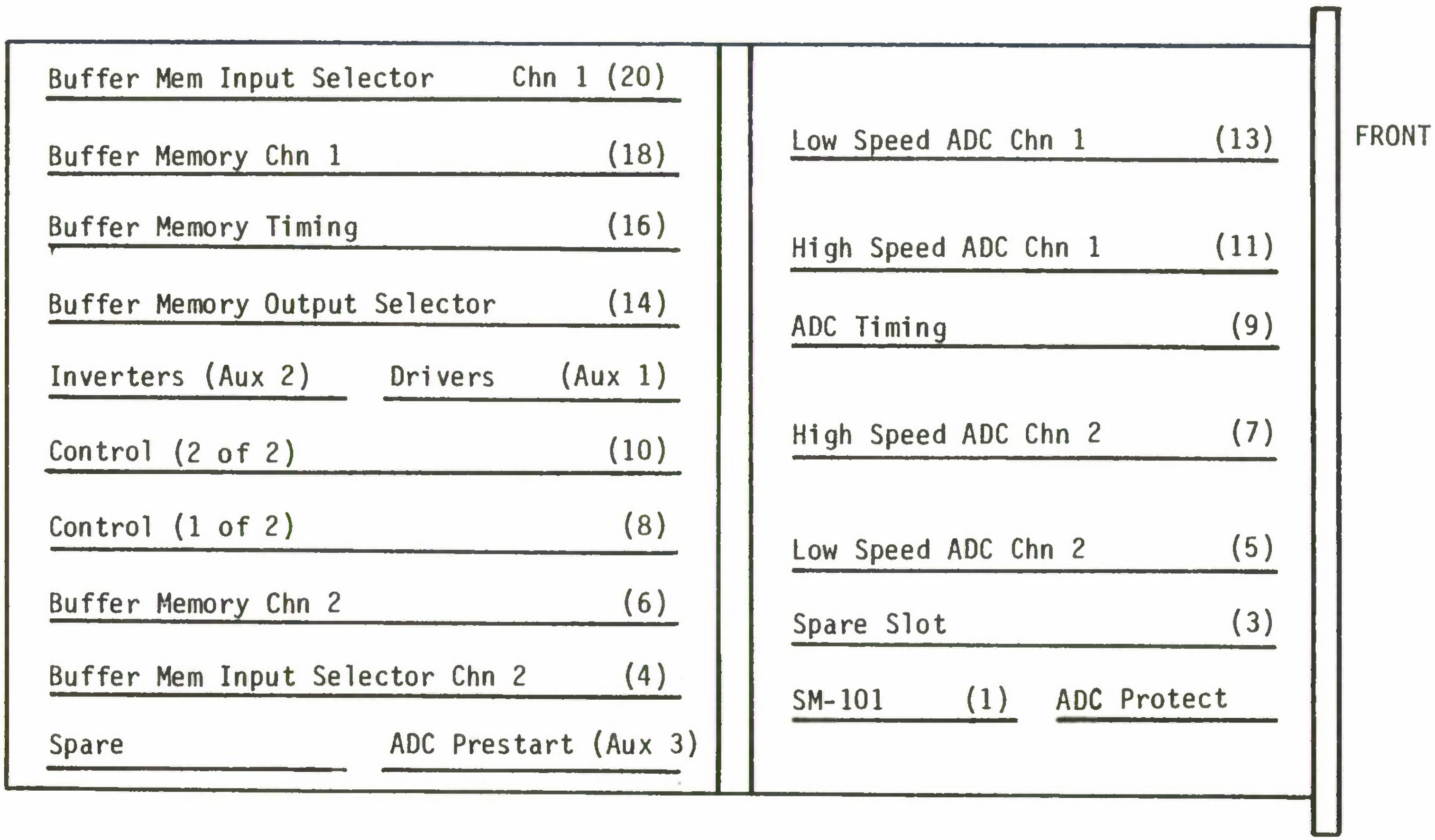



Figure 4. DAU Board Location, Top View DAU

the integrity of those signals and to reduce the stray RF inside the DAU. Where the coaxial cable entered or departed the DAU it was fed through SMA fittings on the back plane, with the exception of the Spectrum Receiver signals that are sent directly to the High Speed ADC boards.

C. DETAILED OPERATION

1. High Speed ADC Board

a. Introduction

The High Speed ADC circuit boards perform six basic functions: 1) high speed analog to digital conversion of the selected signal, 2) Spectrum Receiver (A25) IF down-conversion, 3) selection of down-converted signal from the Spectrum Receiver (A25) or an external baseband signal according to front panel toggle switch setting, 4) baseband signal amplification to appropriate levels for full dynamic range A/D conversion, 5) buffered analog signal to HP-1220 oscilloscope and Rockland filter (eventually to Low Speed ADC boards), and 6) eight bit output data register. Schematic diagram is given in Figure 5.

b. IF Downconversion

Conversion of the Spectrum Receiver IF signal to baseband is accomplished using a MINI-CIRCUITS-LABORATORIES RAY-1 doubly balanced mixer configured as a phase detector. The IF and 30 MHz local oscillator signals from the Spectrum Receiver [Ref. 2] are mixed together and the product low pass

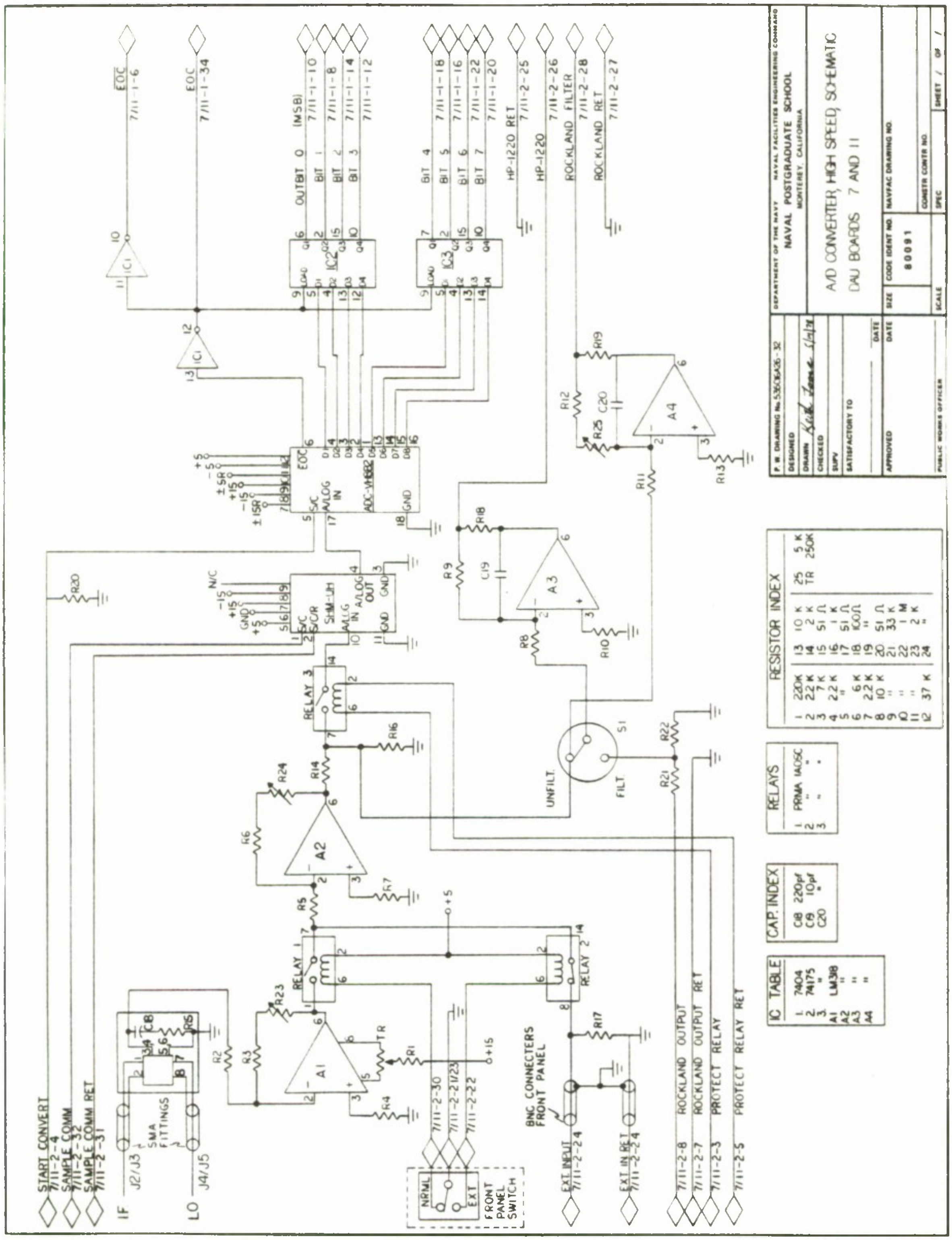



Figure 5 - High Speed ADC Circuit

filtered by the 51 ohm and 22Ø pf RC filter of R15 and C18, to remove the double frequency and residual 3Ø MHz. Operating as a high level mixer (phase detector) with a +13 to +18 dBm local oscillator signal, a peak voltage of approximately 3ØØ mv is available at the input of A1 resistor R2.

c. Baseband Signal Amplification

In order to boost the downconverted signal up to the ADC-VH8B2 modules required full scale voltage of ±1.28 volts, two stages of amplification are provided by LM 318 operational amplifiers A1 and A2. The LM-318 operational amplifier has adequate slew rate and a gain-bandwidth product of 15 MHz. The first stage is limited to a gain of approximately four, in order to maintain a 3 MHz flat bandwidth. Trimpot R23 is used to balance the double balanced mixer output between channel one and channel two as described in Section II.E.4., under ADC dynamic alignment.

The second stage of amplification, A2, in combination with voltage divider R14 and R16, has a gain of approximately one. Trimpot R24 is provided to adjust for full dynamic range as explained in Section II.E.2., static ADC alignment. The three-to-one voltage divider R14 and R15 is utilized to assure overvoltage protection for the SHM-UH module. The SHM-UH can tolerate overvoltage to ±5 volts. Using ±15 volt power on the LM-318 amplifiers the saturation voltage will be no greater than ±13 volts, which divided by 3 is less than ±5 volts. The gain of A2 is approximately three to maintain at least a 3 MHz flat bandwidth.

d. Sample-and-hold Module, DATEL SHM-UH

Analog from amplifier A2 passes through relay 3 to pin 10 of the DATEL Systems, Inc. model SHM-UH 2ØØ picosecond sample-and-hold module. A 7Ø nanosecond sample command signal generated on the ADC Timing board (Section II.C.3.), is supplied to the SHM-UH module pin 1 through edge connector pin 7/11-2-32. The sample command to the SHM-UH module preceeds the start convert command to the A/D converter. This allows the SHM-UH module to have completed the sample-and-hold function prior to the start convert command to the A/D converter. The SHM-UH module has an internal offset trimpot adjustable as explained in the high speed ADC static alignment, Section II.E.2. The analog levels out the SHM-UH module are bipolar, noninverted $\pm$1.28 volt peak levels compatible with the ADC-VH8B2 high speed ADC modules. Performance specifications for the SHM-UH are listed in Appendix 2.

e. Analog-to-Digital Converter Module, DATEL ADC-VH8B2

Stable sample-and-hold levels from the SHM-UH module, directly supplies input to a DATEL Systems, Inc. model ADC-VH8B2 2ØØ nanosecond analog-to-digital converter module. A 4Ø nanosecond start convert pulse is supplied to pin 5 of the ADC-VH8B2 from the ADC Timing board (Section II.C.3.) via edge connector 7/11-2-4.

The end-of-convert (EOC) signal and parallel output data bits D1 through D8 are available 200 nanoseconds after the leading edge of the start convert pulse. The EOC signal is buffered by 7404 inverters in IC-1 and made available for use throughout the DAU as EOC and $\overline{\text{EOC}}$ on edge connector pins 7/11-1-34 and 7/11-1-6 respectively. Additionally EOC from pin 12 of IC-1 is supplied as the load command for the 74175 4 bit latch chips of IC-2 and IC-3. Data bits D1 through D4 are latched in IC-2 and data bits D5 through D8 are latched in IC-3 and made available as output as shown in Figure 5. The parallel data output of the ADC-VH8B2 is offset binary which is converted to two's complement at the buffer registers (IC-2 and IC-3) by complementing bit zero, the most significant bit (MSB). Four calibration trimpots are built into the ADC-VH8B2 module and utilized as explained in the high speed ADC static alignment, Section II.E.2. Performance specifications for the ADC-VH8B2 module are listed in Appendix 2.

f. High Speed ADC Protect Features

The ADC-VH8B2 and SHM-UH modules being both expensive and sensitive to abuse, have been protected by design against 1) overvoltage, and 2) power supply failure. To protect the SHM-UH against inadvertent analog input overvoltage a three-to-one voltage divider formed by R14 and R15, limits the maximum input voltage (even with A2 saturated) to less than $\pm 5$ volts. The output of the SHM-UH module is limited to $\pm 5$ volts which is compatible with the overvoltage limits of the ADC-VH8B2 module.

The power supply failure protect feature, was incorporated due to SHM-UH characteristics discovered during the initial operating period. If analog voltage is applied to the Analog In, of the SHM-UH module without power supply voltages, the module will fail. Relay 3 (CLARE PRMA 1Ø5AB) inline between A2 and the SHM-UH module, can only provide continuity for the analog signal if all DAU power supplies are on and operational, as determined by the ADC Protect Board (Section II.C.5.).

g. ROCKLAND Filter Output

The High Speed ADC board, in addition to supplying downconverted baseband signal or external baseband signal to the high speed ADC module, also provides baseband signal to Low Speed ADC Board. In order to filter the baseband signals to the appropriate passband to prevent aliasing (see digital spectrum discussion Section IV.B.1.) in the spectrum output, A4 provides buffered baseband signal to a ROCKLAND System 816 (A24) digitally controlled multi-channel filter. The filtered output from the Rockland Unit is connected to the Low Speed ADC Boards for higher precision analog-to-digital conversion.

The Low Speed ADC modules require $\pm 5$ volt full scale signals, which requires that a gain of approximately four be derived from A4 (LM318) to bring the $\pm 1.28$ volt full scale input to $\pm 5$ volts. R12 and R11 form the basic gain setting elements of A4 with R25 allowing some gain tolerance for balancing dual channel operation (see Section II.E.3.). R19 and C2Ø form a feedback compensation network to compensate for the capacitive load of the coax cable used to connect to the ROCKLAND filter.

h. HP-122Ø Oscilloscope Output

Continuous input signal monitoring of the SATCOM Signal Analyzer is available through the built in HEWLETT-PACKARD model 122Ø oscilloscope connected via A3 on the High Speed ADC Boards. Amplifier A3 (LM318 operational amplifier IC) is configured similar to A4 with a gain of one determined by R8 and R9. R18 and C19 provide compensation for the capacitive load of the coax cable connecting the HP-122Ø. Switch S1 enables the input to A3 to be switched between an UNFILTERED baseband signal (input to the ROCKLAND filter) or a FILTERED baseband signal (identical to the Low Speed ADC input) brought back onto the board via edge connector pin 7/11-2-8. In this way precise monitoring of the signals supplied to either the high speed ADC modules or the low speed ADC modules can be achieved. Normally the HP-122Ø is operated in the X-Y mode.

i. Front Panel Switches

The selection of desired baseband signal is made on the front panel of the DAU. The NORMAL position activates Relay 1 and deactivates Relay 2 (both CLARE PRMA 1Ø5AB reed relays) to connect Spectrum Receiver (A25) input to the A/D converters. Selection of EXTERNAL deactivates Relay 1 and activates Relay 2 to connect any signal from the front panel input jacks to the A/D converters.

j. Digital Output Data

Eight bits of parallel, two's complement data is available via IC-2 and IC-3, 74175 4 bit latches. Data is updated to IC-2 and IC-3 on each end of convert (EOC) from the ADC-VH8B2 module. Because the data remains available in these latched buffers, present data can be loaded into buffer memory while the next work of A/D converted data is being converted.

k. EOC Signal

The active low end-of-convert signal (EOC) produced by the ADC-VH8B2 at the completion of each conversion, is particularly important to timing synchronization throughout the DAU. Both EOC and $\overline{EOC}$ are available as outputs through buffer inverter gates (74Ø4's) on IC-1.

l. High Speed ADC Timing

Proper timing is particularly critical to the operation of the high speed A/D converters. Figure 6 shows the associated timing configuration.

m. Voltage Requirements

Important to the high performance operation of the DAU, is the cautious use of various power supplies. An important point to note is that separate +15, -15 and +5

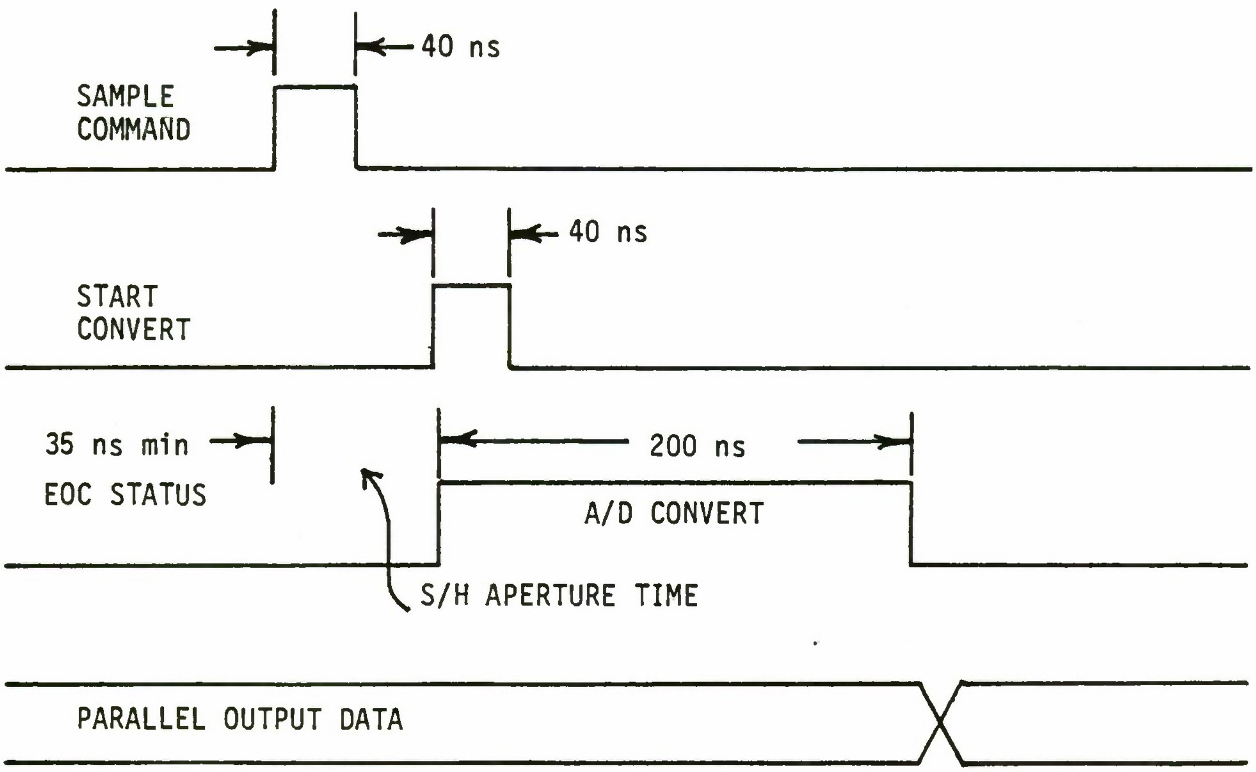



Figure 6 - High Speed ADC Timing Diagram

volt power supplies are used for the channel one low and high speed ADC and S/H modules and amplifiers (DAU boards 11 and 13), and for the channel two low and high speed ADC and S/H modules (DAU boards 5 and 7). Power supplies P18 and P2Ø are dedicated to the channel one boards, while power supplies P19 and P21 are dedicated to the channel two boards. This technique assures maximum isolation between channel one and channel two to avoid any cross talk ambiguities. One additional power supply, P17, is common to both the channel one and channel two ADC-VH8B2 module to provide -5 volts. This requirement is a low power requirement, not considered to be a cross talk contributor. Power supplies P17, P2Ø and P21 are physically mounted on the back plane of the DAU. All remaining DAU power supplies are mounted in the rear of equipment racks 16 and 17. The additional power supplies include ±15 volts to the LM-318 operational amplifiers, and +5 volts to the TTL logic IC's.

n. Component Layout

Figure 7 shows the major component layout in the High Speed ADC Boards.

2. <u>Low Speed ADC Board</u>

a. Introduction

Data Acquisition Unit boards 13 and 5 provide 12 bit analog-to-digital conversion for channel one and channel two data respectively. Unlike the more complicated High Speed ADC boards, the Low Speed ADC boards perform only two functions.

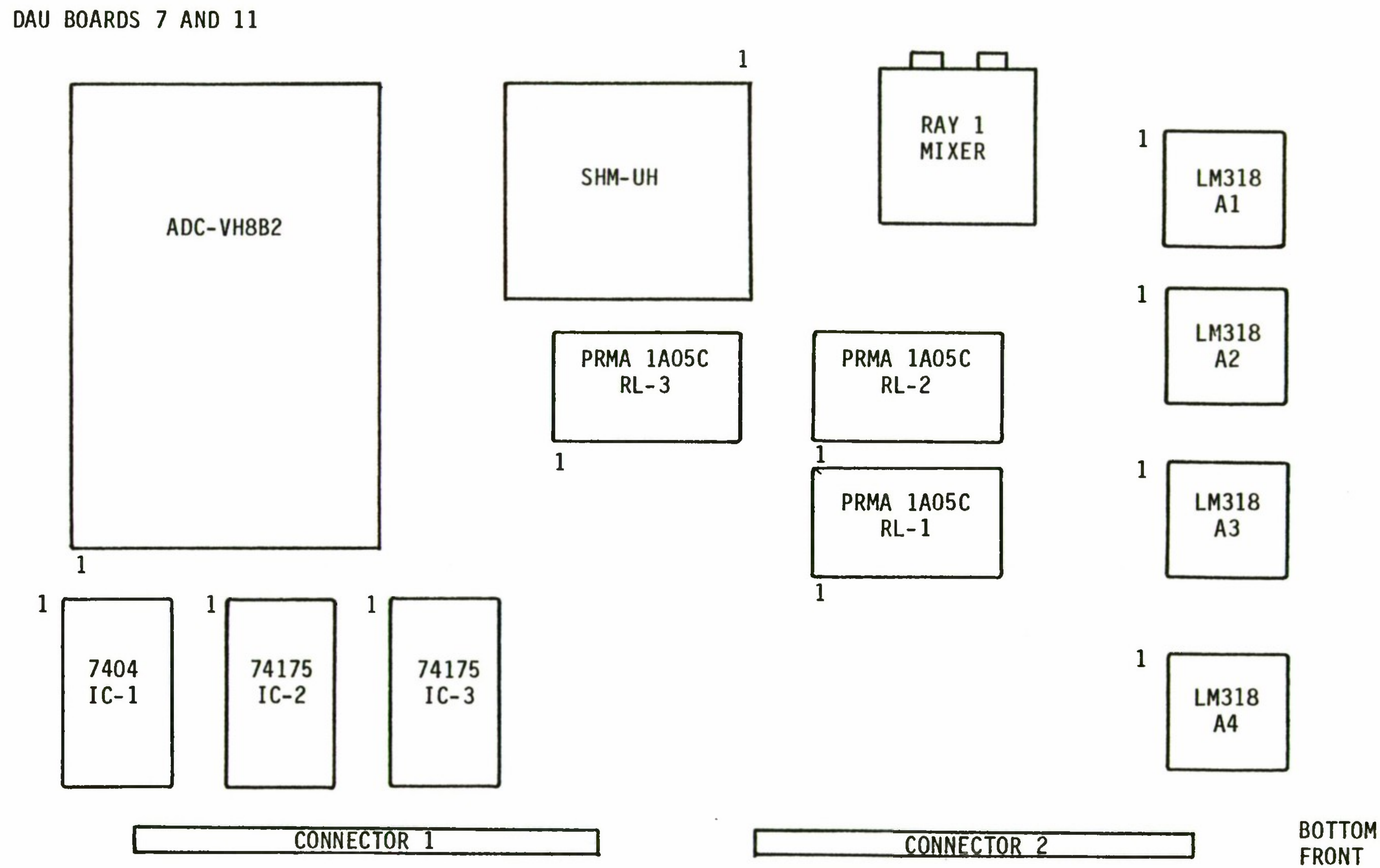



Figure 7. High Speed ADC Component Layout

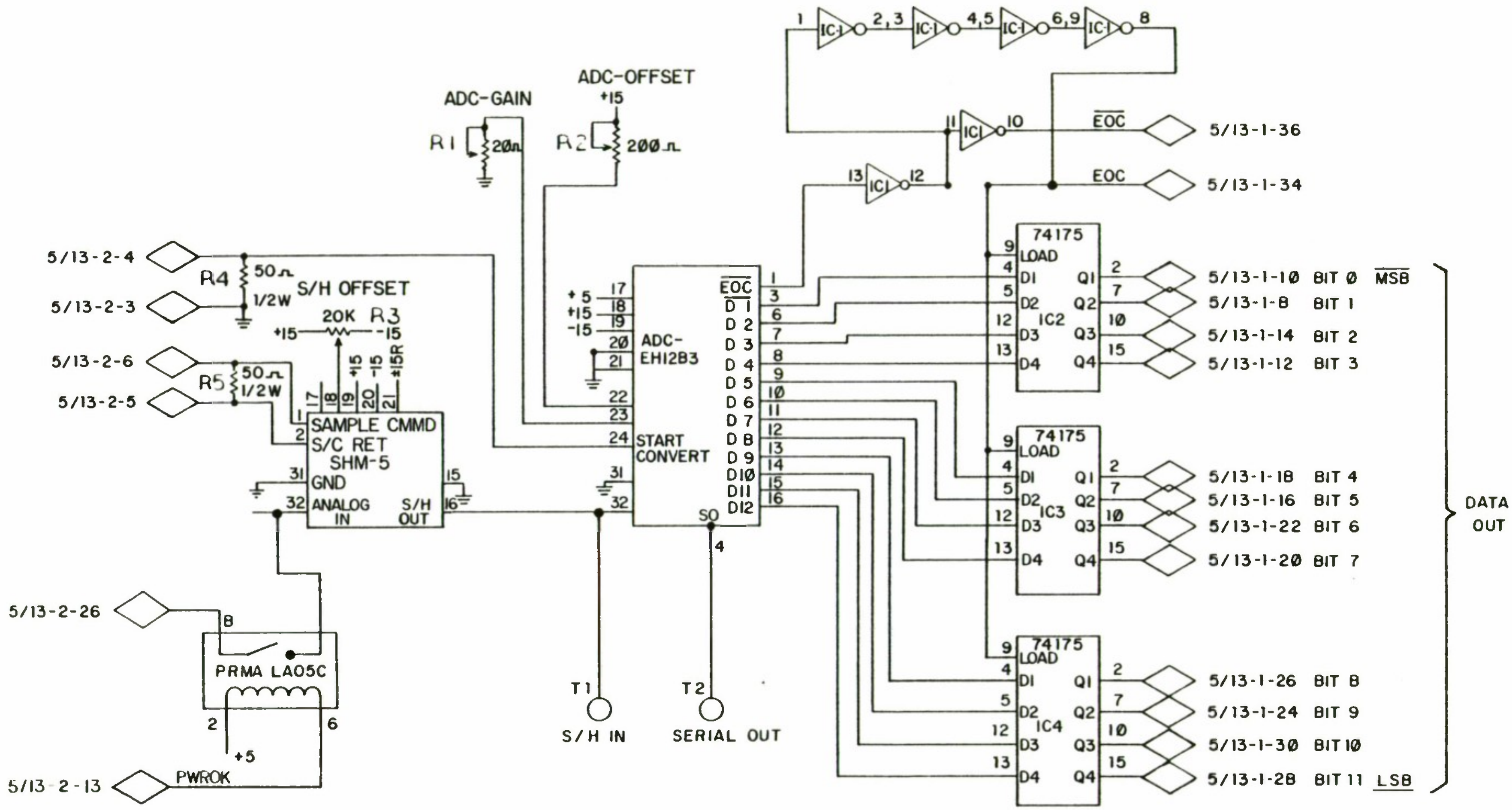
First, filtered baseband signal from the ROCKLAND System 816 filter is converted to digital data, and second, the converted two's complement data is latched in a buffer register for transfer to buffer memory. The schematic diagram is given in Figure 8.

b. Sample-and-Hold Module, DATEL SHM-5

Analog baseband signal from the ROCKLAND System 816 digitally controlled filter is converted to stable levels between ±5 volts peak-to-peak by the DATEL Systems, Inc. model SHM-5 2ØØ nanosecond sample-and-hold module. A 32Ø nanosecond sample command signal generated on the ADC Timing board (Section II.C.3.), is supplied to the SHM-5 module pin 1 via edge connector pin 5/13-2-6. To assure a stable signal level for A/D conversion, the sample command preceeds the start convert pulse to the A/D converter. The SHM-5 module uses a 2ØK ohm external trimpot to provide offset adjustment as explained in Section II.E.3., Low Speed ADC alignment. The analog levels out of the SHM-5 module are bipolar, inverted ±5 volt peak levels compatible with the ADC-EH12B3 A/D converter module. Performance specifications for the SHM-5 are listed in Appendix 2.

c. Analog-to-Digital Conversion Module, DATEL ADC-EH12B3

Stable sample-and-hold levels from the SHM-5 are directly sent to the DATEL Systems, Inc. model ADC-EH12B3 2 microsecond, 12 bit analog-to-digital converter. A 1ØØ




SET FOR TWO'S COMPLIMENT MODE
I. E. $\overline{\text{MSB}}$ IS USED FROM ADC-EH12B3

◇ EDGE CONNECTOR PIN

○ TEST PIN

Figure 8 - Low Speed ADC Circuit

nanosecond start convert pulse generated on the ADC Timing board (Section II.C.3.) is supplied to the ADC-EH12B3 module pin 24 via edge connector pin 5/13-2-4. The end-of-convert (EOC) signal and parallel output data bits D1 through D12 are available 2 microseconds after the leading edge of the start convert pulse. The ADC-EH12B3 module also provides serial output data available at pin 4. The serial out signal and sample-and-hold out signal are conveniently made available at test points T2 and T1 respectively. The EOC signal is buffered by 74Ø4 inverters in IC-1 and made available for use throughout the DAU as EOC and $\overline{\text{EOC}}$ on edge connector pins 5/13-1-34 and 5/13-1-36. Additionally IC-1 pin 12 is utilized as the load command for the output data buffer-latch register, IC-2, IC-3 and IC-4. The parallel data output of the ADC-EH12B3 is two's complement. This option is made available by utilizing the complement of bit zero, pin 3, the most significant bit (MSB). A 2Ø ohm calibration trimpot for ADC GAIN and a 200 ohm calibration trimpot for ADC-OFFSET are provided externally to be utilized as per the low speed ADC static alignment, Section II.E.3. Performance specifications for the ADC-EH12B3 module are listed in Appendix 2.

d. ADC Protect Features

The ADC-EH12B3 and SHM-5 modules, being both expensive and sensitive to abuse, have been protected by design against 1) overvoltage, and 2) power supply failure. The overvoltage limit for the SHM-5 module is ±15 volts which is greater than the saturation voltage of amplifier A4 on the High Speed ADC board, where the low speed ADC baseband signal originates. The overvoltage limit for the ADC-EH12B3 module is ±15 volts which again is greater than the saturation level of the SHM-5 module output. The power supply failure protect feature, was incorporated to protect the SHM-5 module against the application of an analog signal while the SHM-5 power supply voltages are off, a failure-producing condition. A CLARE PRMA 1AØ5C reed relay is used between the analog input signal on pin 5/13-2-26 and the SHM-5 analog input, pin 32. The relay can only provide signal continuity if all DAU power supplies are operational, a condition monitored on the ADC Protect Board (Section II.C.5.).

e. Digital Output Data

Twelve bits of parallel, two's complement data is available via IC-2, IC-3 and IC-4, 74175 4 bit latches. Data is updated to these latches on each EOC from the ADC-EH12B3 module. Because data remains available in these latched buffers during conversion time present data can be loaded into buffer memory while the next word of A/D converted data is being converted.

f. EOC Signal

The active low end-of-convert signal ($\overline{\text{EOC}}$) produced by the ADC-EH12B3 at the completion of each conversion, is particularly important to timing synchronization throughout the DAU. EOC and $\overline{\text{EOC}}$ versions are available as output through buffer inverter gates (74Ø4's) on IC-1. EOC is additionally put through four more inverter gates on IC-1 to provide approximately 28 nanoseconds of delay to assure that the data has been latched and stabilized before using loaded into buffer memory.

g. Low Speed ADC Timing

Figure 9 shows the timing configuration associated with the Low Speed ADC board.

h. Voltage Requirements

For a discussion of voltage requirements for the Low Speed ADC boards see Section II.C.1.m.

i. Component Layout

Figure 1Ø shows the major component layout for the Low Speed ADC boards.

3. <u>ADC Timing Board</u>

a. Introduction

The ADC Timing circuit, DAU board 9 shown in Figure 11, performs four basic functions. It 1) precisely generates correctly timed high or low speed sample command pulses, 2) precisely generates correctly timed high or low speed start convert pulses, 3) buffers the generated pulses with appropriate bus drivers, and 4) selects whether to generate high speed or low speed timing pulses.

b. Sample Command Pulse

The 32Ø nanosecond sample command for low speed A/D conversion is generated by IC-8, a 74121 monostable

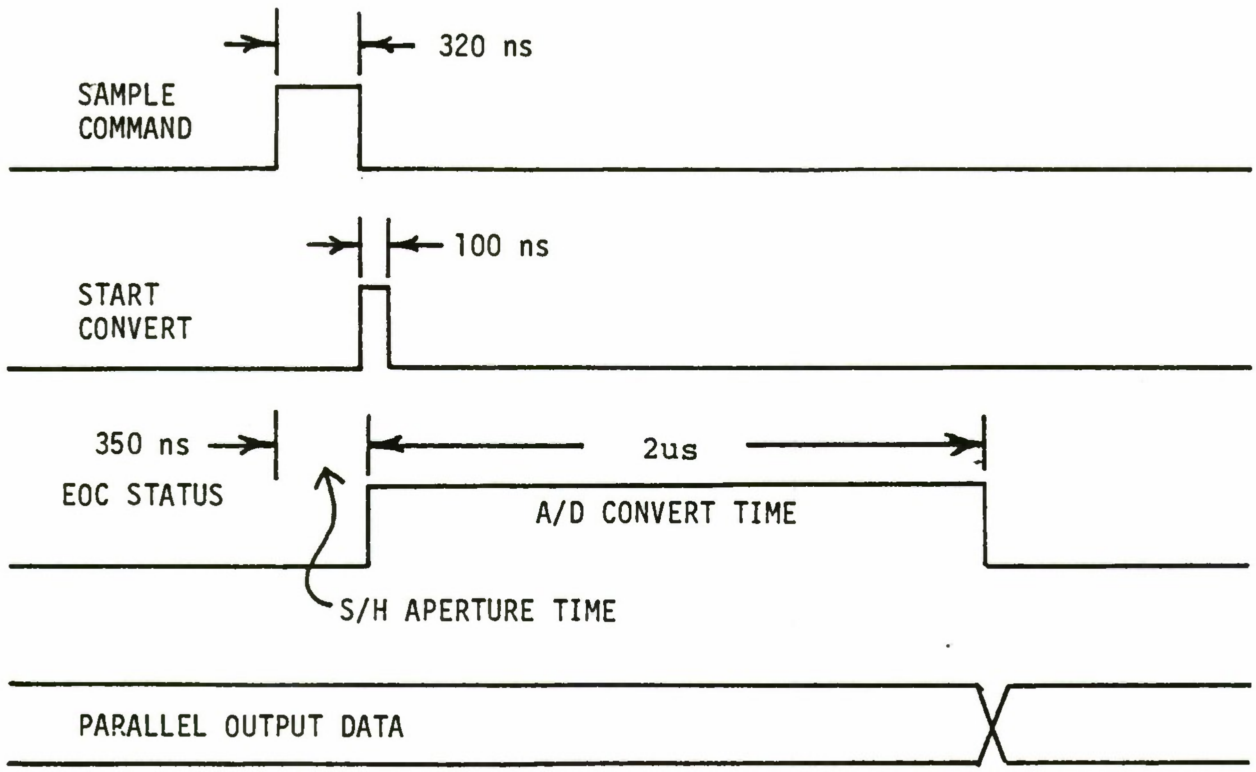



Figure 9 - Low Speed ACD Timing Diagram

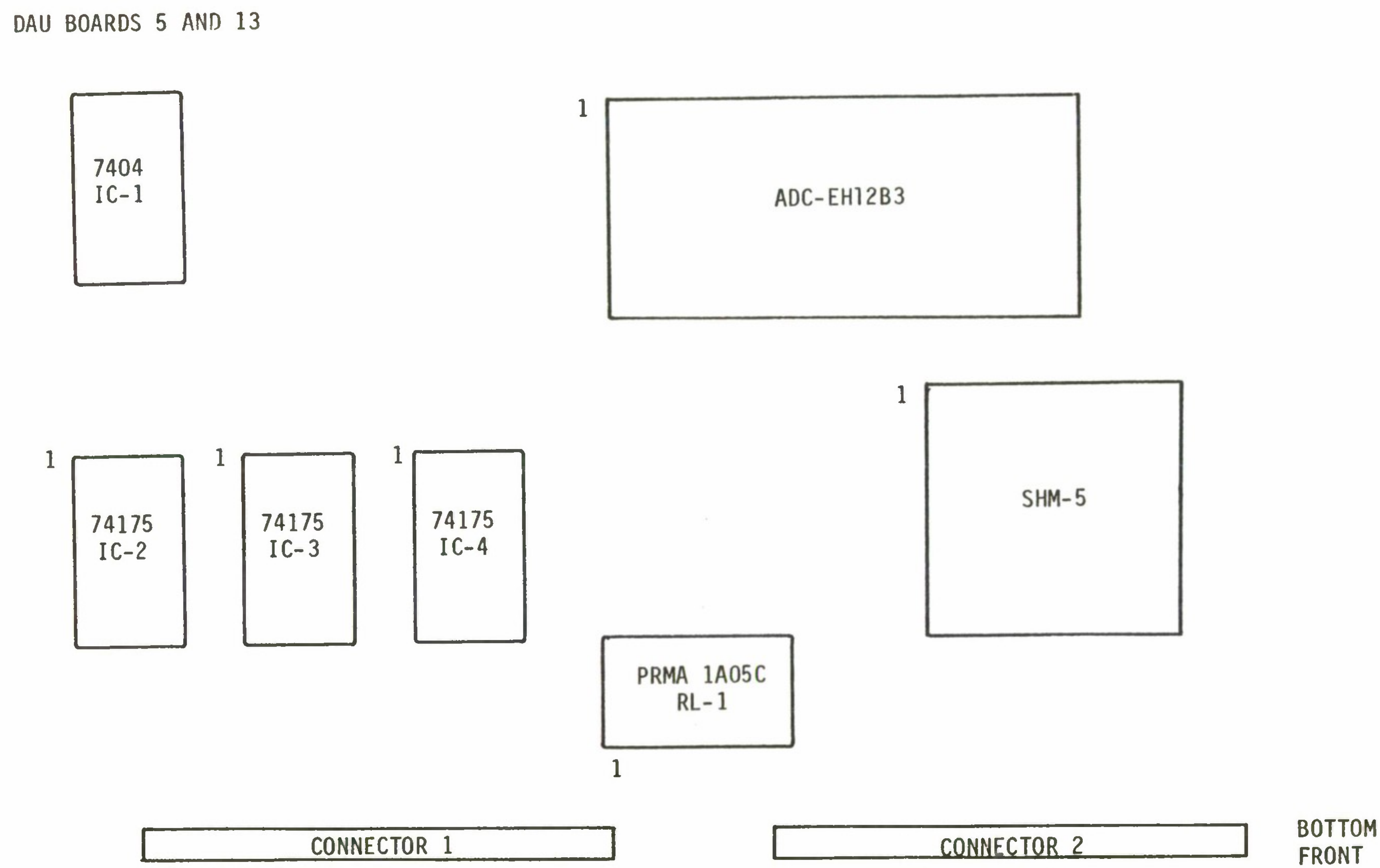



Figure 10. Low Speed ADC Component Layout

multivibrator. Input clock SYNTEST 2 (from the ADC Prestart circuit, Section II.C.4.) inverted by a 74Ø4 gate on IC-3 triggers IC-8 on the high to low transition on pins 3 and 4, provided it is enabled with a high on pin 5. Output Q, pin 6, a positive pulse is used to trigger the start convert pulse in IC-7. Output $\overline{Q}$, pin 1, a negative pulse is sent to bus driver gates on IC-2. The 32Ø nanosecond pulse length is determined by the 2Ø ohm resistor, 22 picofarad capacitor combination attached to IC-8. The 4Ø nanosecond high speed sample command pulse is generated on the 74121, IC-1Ø, just as was the low speed pulse with the enable signal on pin 5 controlled separatly from the low speed enable. The Q output is used to trigger the start convert pulse in IC-11 and $\overline{Q}$ is sent to bus driver gates on IC-4 and IC-5.

c. Start Convert Pulse

The 1ØØ nanosecond start convert pulse for low speed A/D conversion is generated in IC-7 while the high speed start convert pulse is identically generated in IC-11. Both pulses are generated on the high-to-low transition of the trailing edge of the respective sample command, applied to pins 3 and 4 of the 74121's. Both 74121's have the enable, pin 5, tied high to allow a pulse to be triggered whenever a sample command has been generated. The low speed start convert negative pulse on $\overline{Q}$, pin 1 of IC-7, is sent to bus driver gates on IC-1. The high speed start convert negative pulse on $\overline{Q}$, pin 1 of IC-11 is sent to bus driver gates on IC-1.

d. Bus Driver Outputs

Consideration to simultaneous dual channel A/D conversion is given throughout the DAU design. To assure minimum possible phase error of sample command and start convert pulses for channels one and two, each output pulse is individually buffered by high speed Schottky TTL 74S14Ø bus driver gates. The dual channel pulses out of the bus drivers are sent to the output edge connector pins through identical length printed circuit runs and then sent to the ADC converter boards through 5Ø ohm coaxial transmission line.

The output pulses for each signal are configured identically as shown in Figure 11, with the exception of the sample command for the high speed ADC boards. To assure a clean fast rise leading edge on this set of pulses two 74S14Ø gates, IC-4 and IC-5, were used in parallel with external 1ØØ ohm pull up resistors.

e. ADC Selection

Depending on control signals ADC2-LO and ADC2-HI, from the ADC Prestart circuit Section II.C.4., either or both high or low speed sample command and start convert pulses can be enabled. Normally (depending on software) only the high or low speed pulses would be generated. When ADC2-LO is asserted high via edge connector pin 9-1-31, it brings the D input, pin 2, of the 7474 gate on IC-9 high and simultaneously removes the active low direct clear from pin 1. Coincident with the first low to high transition of the SYNTEST2 clock, through

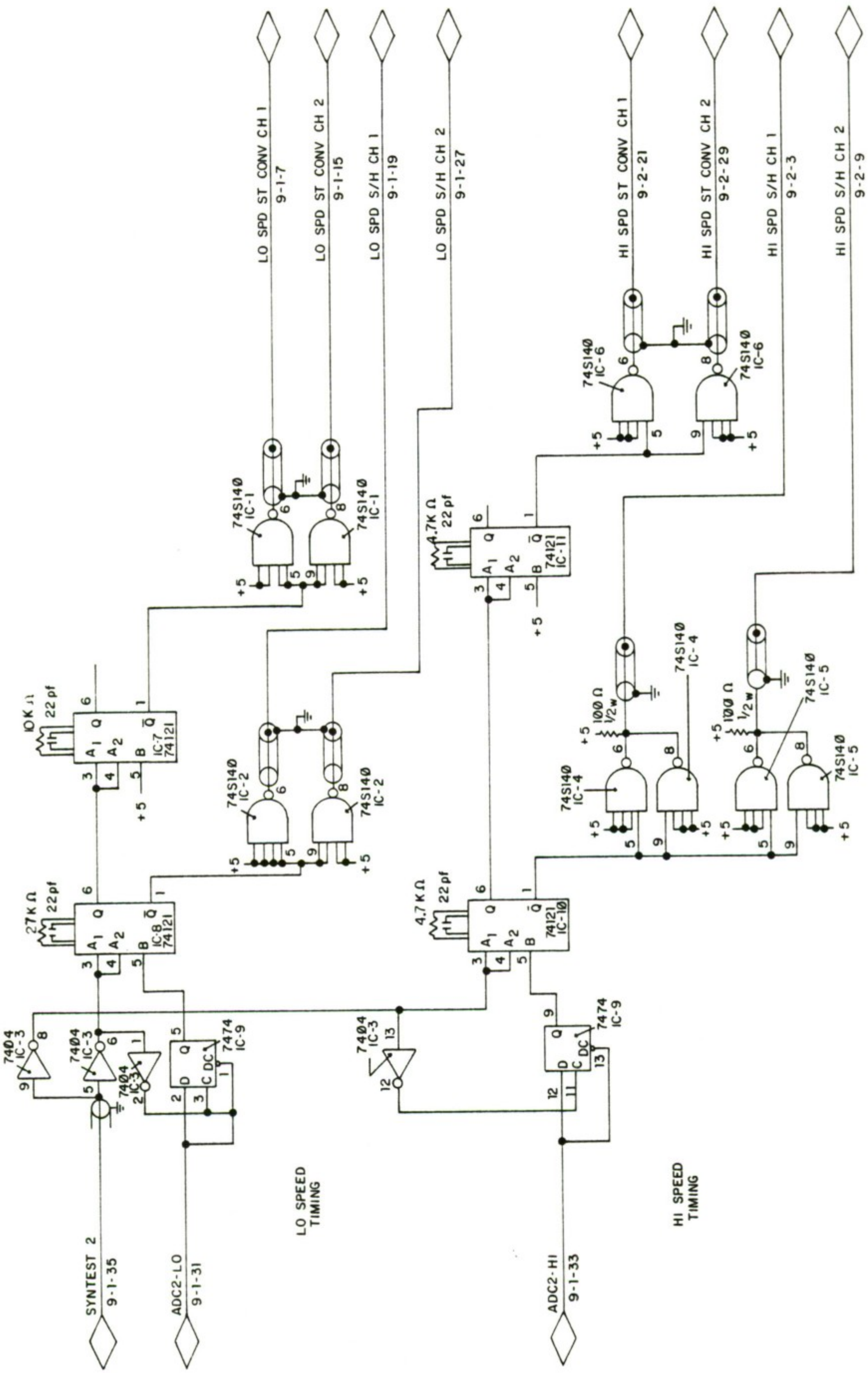



Figure 11 - ADC Timing Circuit

inverters on IC-3, the Q output, pin 5, goes high to enable the 74121, IC-8, pin 5. The sample command one shot is triggered on the next clock cycle. The high speed half of the circuit is implemented in the exact same manner controlled by ADC2-HI via edge connector pin 9-1-33 to D flip-flop 7474, pin 12 on IC-9.

f. ADC Timing Circuit Timing Diagram

Figure 12 shows the complete ADC circuit timing sequence. Table I shows A/D conversion and ADC Timing Signal.

g. Voltage Requirements

Plus 5 volt power is supplied to the ADC Timing board, DAU board 9 from the main logic power supply P16 located in the bottom rear of equipment rack 16.

h. Component Layout

Figure 13 shows the major component layout for the ADC Timing Circuit board.

4. ADC Prestart Board

a. Introduction

The ADC Prestart circuit, DAU auxiliary board 3, Figure 14, was designed and implemented to circumvent a characteristic limitation of the DATEL sample-and-hold modules. If the SHM-5 module is suppled DC power with no sample command pulses applied, the output level drifts to its saturation level of approximately $\pm 14$ volts. When the sample command pulses are then applied, a period of time must pass before the output level is correct. This limitation causes the obvious

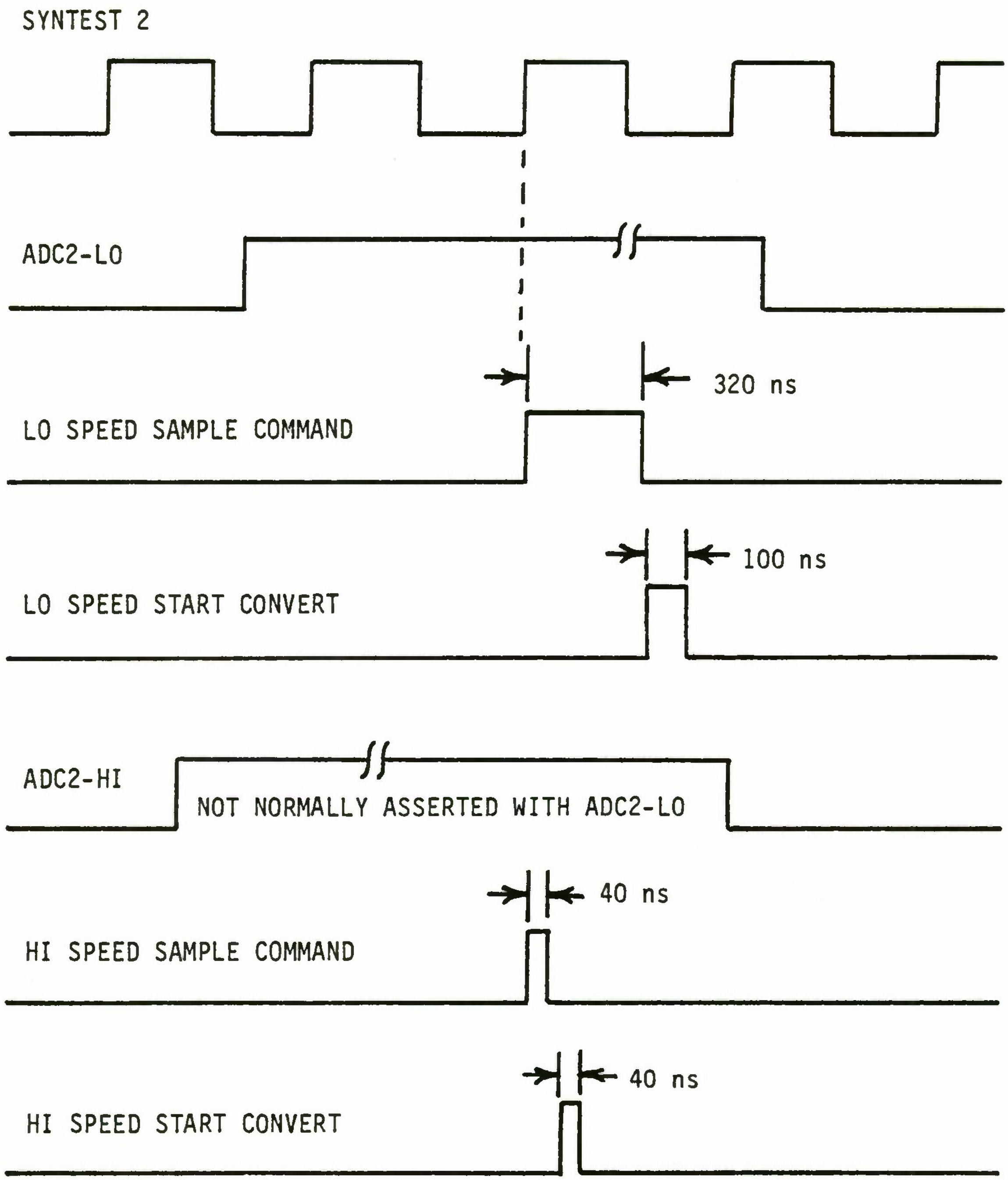



Figure 12. ADC Timing Circuit Timing Diagram

Table I - ADC Conversion and ADC Timing Signals

| SIGNAL NAME | SOURCE | DESTINATION | PURPOSE | REF(page) |
|---|---|---|---|---|
| Low Speed Sample Comm | ADC Timing Bd | Low Speed ADC Bds | Start Sample | Sec II.C.3.b. |
| Low Speed Start Conv | ADC Timing Bd | Low Speed ADC Bds | Start Conversion | Sec II.C.3.c. |
| High Speed Sample Comm | ADC Timing Bd | High Speed ADC Bds | Start Sample | Sec II.C.3.b |
| High Speed Start Conv | ADC Timing Bd | High Speed ADC Bds | Start Conversion | Sec II.C.3.c |
| EOC Chn 1 Low | Low Spd ADC, Chn 1 | Buffer Memory | Indications | Sec II.C.2.f. |
| EOC Chn 2 Low | Low Spd ADC, Chn 2 | Timing Bd, | end of A/D | Sec II.C.2.f |
| EOC Chn 1 High | High Spd ADC, Chn 1 | Control Board (1 of 2) | conversion | Sec II.C.1.k. |
| EOC Chn 2 High | High Spd ADC, Chn 2 | | | Sec II.C.1.k. |
| PWROK | ADC Protect Bd | All 4 ADC Boards | Indicates all power supplies operational | Sec II.C.5.d. |

DAU BOARD 9

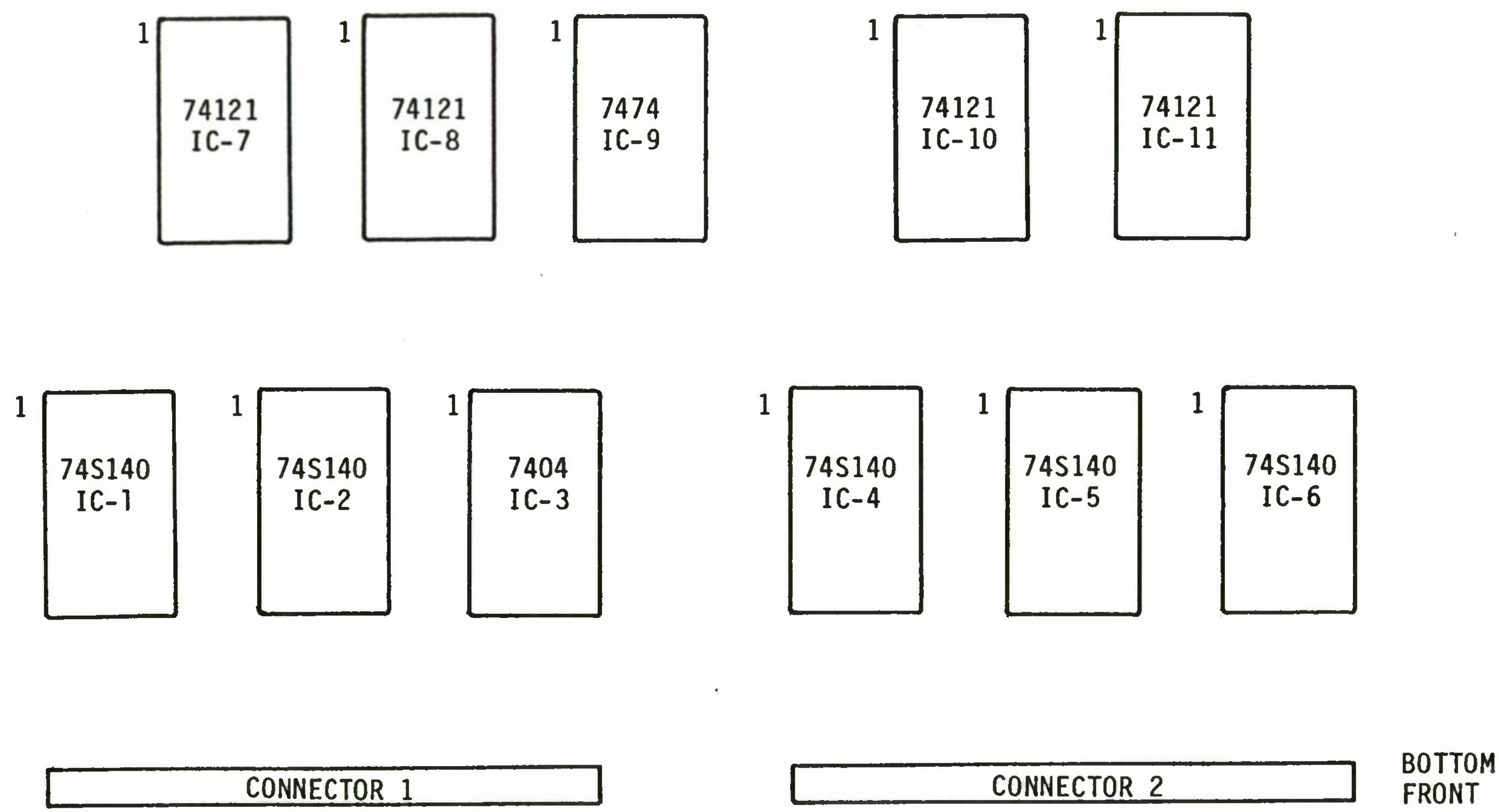



Figure 13. ADC Timing Board Component Layout

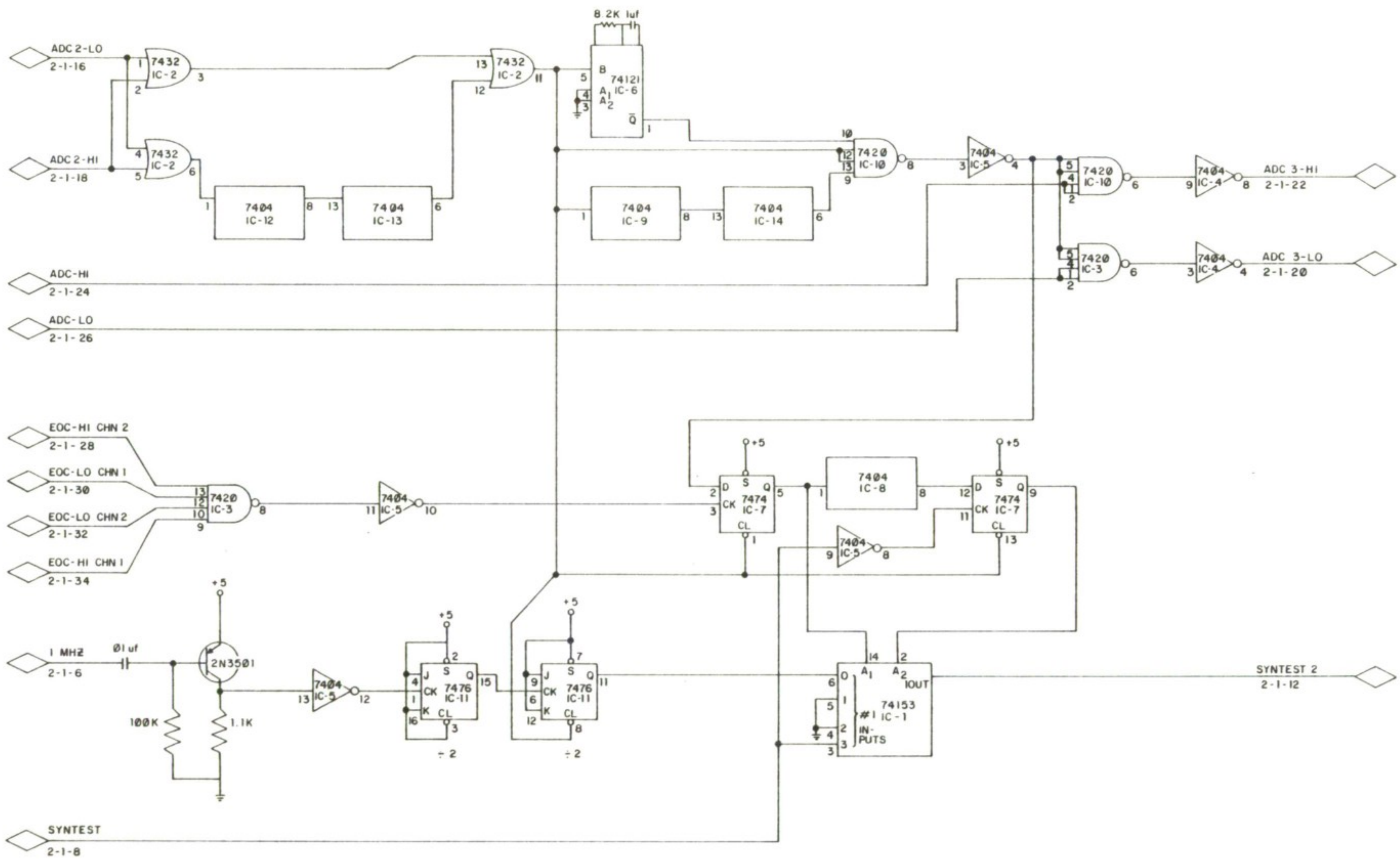



Figure 14 - ADC Prestart Circuit Auxiliary Board 3

problem of inaccurate A/D data throughout this correction time period. To correct this problem, the desired ADC circuit is started and operated for approximately 2 milliseconds before valid data acquisition is begun. A 74121 monostable multivibrator is used to establish the 2 millisecond delay and control prestart circuit changes. A 1 MHz frequency standard signal, divided by four, provides a 250 KHz clock rate to operate the selected ADC circuit during the prestart 2 millisecond time-out period. Then the clock rate is smoothly transitioned by a four-to-one multiplexer, to the desired sample rate as determined by the SM-101 frequency synthesizer. Valid data acquisition is then possible for as many blocks of data acquisition as desired using the ON ADC boards. Prestart does not have to be re-initiated for changes in sample rate within the limits of the ON ADC's. When the OFF ADC's are to be used, the prestart sequence must take place to bring the OFF ADC's to an operational state. It is not possible to leave both high and low speed ADC's ON at all times due to the possibility of sample rates outside the range of the low speed ADC's. This circuit generates ADC3-HI, ADC3-LO and SYNTEST 2.

b. ADC3-HI, ADC3-LO Output Signals

The ADC3-HI and ADC3-LO active high output signals are generated by the ADC prestart circuit and sent to the Buffer Memory Timing Circuit (Section II.C.8.) where they enable data storage for the operational A/D converter.

Starting from a condition with neither the high nor low speed A/D converters on, both ADC3 signals low, circuit operation can be traced through Figure 14 as follows: When either ADC2-LO or ADC2-HI inputs on edge connector pins 2-1-16 or 2-1-18 is asserted high by the Control Board (2 of 2), Section II.C.13, it is basically OR'ed through 7432 gates on IC-2 and applied to the 74121, pin 5, on IC-6 triggering a 2 millisecond prestart delay pulse. The requirement for IC-12 and IC-13 is explained in Section II.C.4.d. The output of IC-6 taken from $\overline{Q}$, applies a 2 millisecond active low gate to a 7420 NAND gate, IC-2Ø. To prevent start up glitches the prestart delay pulse is NAND'ed in IC-20 with the OR'ed ADC2 signal and a delayed version of the OR'ed ADC2 signal. This arrangement allows either ADC3 signal to only be high when the corresponding ADC2 signal has been applied and after the prestart delay. IC-9 and IC-14 provide approximately 12Ø nanoseconds of delay to prevent the 742Ø output, pin 8 IC-1Ø, from momentarily going low before the prestart delay brings it back high during its pulse duration.

At the trailing edge of the prestart delay pulse all inputs to the 742Ø, IC-1Ø are high allowing the output pin 8 to go low and remain low for as long as the asserted ADC2 signal remains. Inverting this output with the 74Ø4 gate, pin 4 IC-5 provides a high signal to two more 742Ø NAND gates on IC-3 and IC-1Ø. When either the ADC-HI or ADC-LO input signals, edge connector pin 2-1-24 and 2-1-26, coming from

Control Board (2 of 2) is asserted high, its corresponding 7420 NAND gate goes low, is inverted and ADC3-HI or ADC3-LO is asserted. Subsequently removing and reasserting the ADC3 signal off or on again can be done without reinitiating the prestart time delay. The SYNTEST 2 output signal must be considered in order to understand the entire function of the prestart delay pulse.

c. SYNTEST 2 Output Signal

The SYNTEST 2 Output provides rectangular clock cycles applied to the ADC Timing Board (Section II.C.3.) for synchronization of the operational A/D converter. SYNTEST 2 will be in one of three states, either off (low), on at a 25Ø KHz prestart frequency or at the selected ADC sample rate determined by the SM-101 frequency synthesizer. Starting from the off condition (SYNTEST low and ADC2-HI, ADC2-LO low), circuit operation can be traced through Figure 14 as follows: A 1 MHz sine wave, supplied from the frequency distribution amplifiers in equipment rack 18, brought in through edge connector pin 2-1-6, is converted to a TTL square wave by the 2N35Ø1 transistor, Q1, operating as a saturating switch. Q1's output buffered by a 74Ø4 inverter on IC-5 is divided down to 250 KHz, the toggle action of two J-K flip-flops on IC-11. The output from the second J-K flip-flop, pin 11, IC-11, is disabled and remains low while the clear input, pin 8, is held low by the ADC2-OR signal, pin 11, IC-2, corresponding to the SYNTEST 2 off state. When either ADC2 signal is asserted (see Section II.C.4.b.) 250 KHz from IC-11, pin 11 is applied to the zero input of a 74153 four-to-one multiplexer, pin 6, IC-1. In the prestart condition specified, both addresses of IC-1 are low causing the output pin 7, which is SYNTEST 2, to operate at the 250 KHz clock rate. Hence, by the application of ADC2-HI or ADC2-LO either the high or low speed ADC boards have been started at 250 KHz, a sample rate useable by either set of A/D converters. Also note that the operational A/D converters will now be sending out end-of-convert (EOC) signals which are used as feedback signals for follow-on stages of operation.

At the same time the ADC2-OR signal enabled the 250 KHz clock, it triggered the prestart delay pulse and removed the clear input from the two D flip-flops on IC-7, pins 1 and 13. At the trailing edge of the prestart delay pulse, inverter output pin 4 of IC-5 goes high and is applied to the first D flip-flop pin 2, IC-7. Two EOC's either high speed or low speed, operating at the 250 KHz prestart frequency, propagates through the 7420 NAND gate IC-3, and 7404 inverter IC-5 to be applied to the clock input pin 3 of the first D flip-flop. On the positive transition of that EOC input the Q output pin 5 goes high, applying a "1" to address A1 of the multiplexer IC-1, pin 14. This moves the multiplexer's output to the "1" input which is grounded, causing SYNTEST 2 to stay low. Simultaneous with this multiplexer change the high on pin 5 of IC-7 starts propagating through a 60 nanosecond delay created by 6 74Ø4 gates on IC-8. After 6Ø nanoseconds the D input, pin 12, IC-7, of the second D flip-flop is brought high. Coincident with the positive transition of the SYNTEST clock input, from the SM-101, the Q output pin 9 goes high to change the address A2 of the multiplexer to "1". Now multiplexer input "3" is selected to put the SYNTEST sample rate on the SYNTEST 2 Output. Note that the SYNTEST input to the multiplexer is 18Ø degrees out of phase with the address A2 change, by the action of inverters 7404 on IC-5. This assures that the first positive edge on the SYNTEST 2 at the SYNTEST frequency occurs cleanly after input "3" has been selected.

d. ADC Prestart Timing

The timing relationships for the ADC Prestart circuit are shown in Figure 15. To protect this circuit from possible inaccurate operation as the ADC2-LO and ADC2-HI inputs were switched, additional logic was included (two additional 7432 OR gates, on IC-2, and two 74Ø4 hex inverter chips, IC-12 and IC-13 for delay) to make up the ADC2 or function. This configuration assures that the B input of the 74121 monostable multivibrator, pin 5 IC-6, will remain high if ADC2-LO and ADC2-HI are switched to opposite states simultaneously. This avoids a possible partial reset of the ADC Prestart circuitry (a condition that could cause improper DAU operation), but requires that software control be used to allow a new prestart sequence when switching to the unused

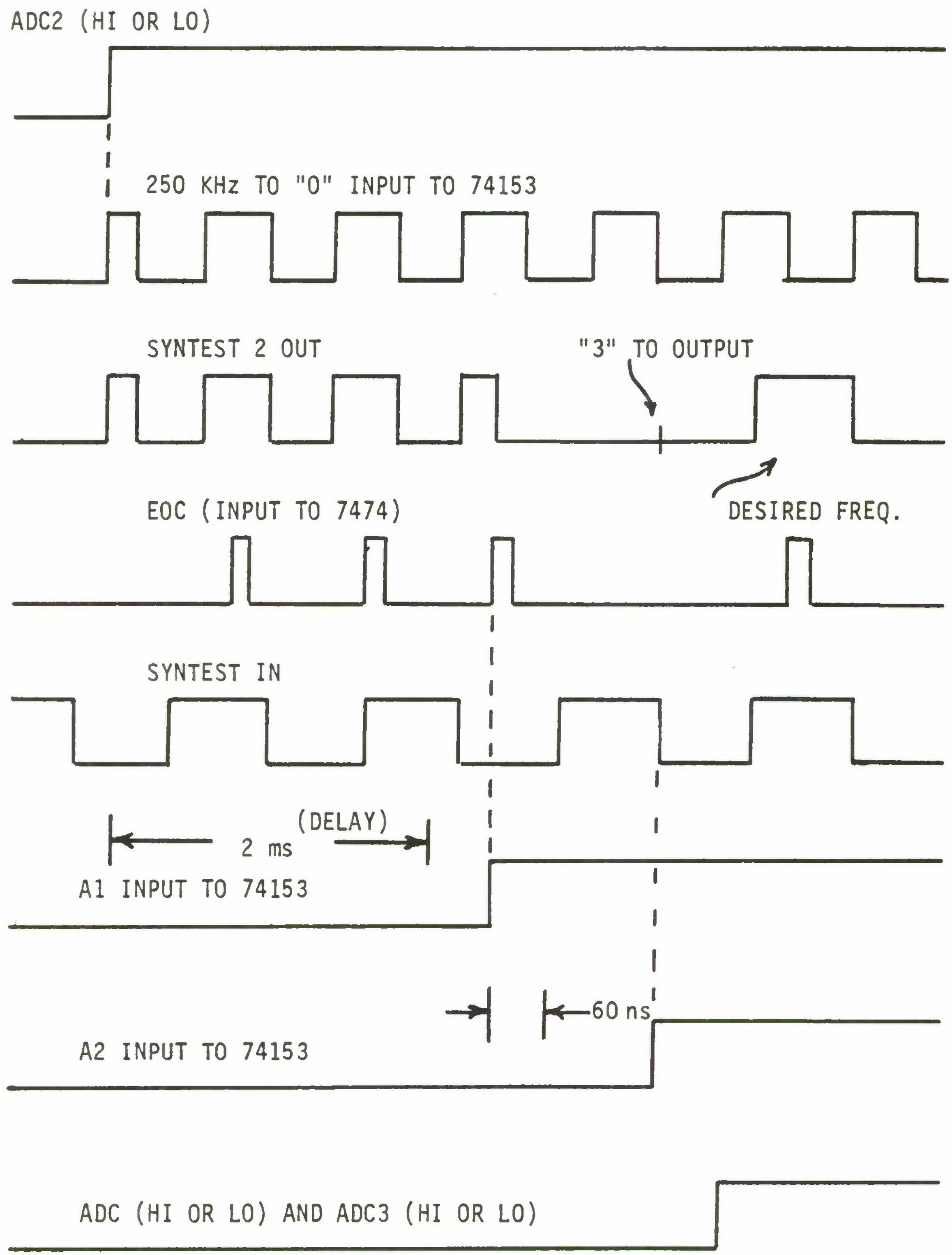



Figure 15. ADC Prestart Circuit Timing Diagram

TABLE II. ADC PRESTART SIGNALS

| Signal Name | Source | Destination | Purpose | Ref (Page) |
|---|---|---|---|---|
| ADC2-LO | Control Board (2 of 2) | ADC Prestart Bd, ADC Timing Bd | Initiate Prestart Sequence | Sec II.C.13.h |
| ADC2-HI | | | | |
| ADC-LO | | ADC Prestart Bd, Inverter Bd | Enable ADC3-HI/LO | |
| ADC-HI | | | Create ASEL/BSEL | |
| ADC3-LO | ADC Prestart Bd | Buff Mem Timing Bd | Allow Data Acquisition | Sec II.C.4.b. |
| ADC3-HI | ADC Prestart Bd | Buff Mem Timing Bd | | Sec II.C.4.b. |
| SYNTEST | SYNTEST 101 | ADC Prestart Bd | Generate SYNTEST2 | Sec II.C.4.c. |
| 1MHZ | External Distr Ampl | ADC Prestart Bd, SM101 Bd | Generate 250 KHz | Sec II.C.4.c. |
| 250 KHz | ADC Prestart Bd | ADC Timing Bd | Prestart Freq | Sec II.C.4.c. |
| SYNTEST2 | ADC Prestart Bd | ADC Timing Bd | Final Freq | Sec II.C.4.c |

ADC boards. Table X specifies the proper software control. Table II lists all ADC Prestart associated signals.

e. Voltage Requirements

The ADC Prestart circuit utilized main logic +5 volt power from supply P16 located in equipment rack 16, lower reat.

f. Component Layout

Figure 16 shows the major component layout for the ADC Prestart board.

5. <u>ADC Protect Circuit Board</u>

a. Introduction

During the initial design phase it was discovered that the DATEL analog-to-digital and sample-and-hold modules could be damaged by applying an analog signal while the power supplies were off. This condition, which could arise from a power supply failure or incorrect power down sequence, could not be tolerated for these modules. To protect against the above possibility, and to visually represent the status of all DAU power supplies, the ADC Protect circuit was designed and implemented as auxiliary board 4. The ADC Protect Circuit, Figure 17, consists of ten reed relays and ten light-emitting diodes (LED'S).

b. PRMA 1Ø5C Relays

Each separate power supply that provides power to the DAU is brought onto the ADC Protect board and current limited as necessary to pull-in an individual CLARE PRMA 1Ø5C

DAU AUXILIARY BOARD 3

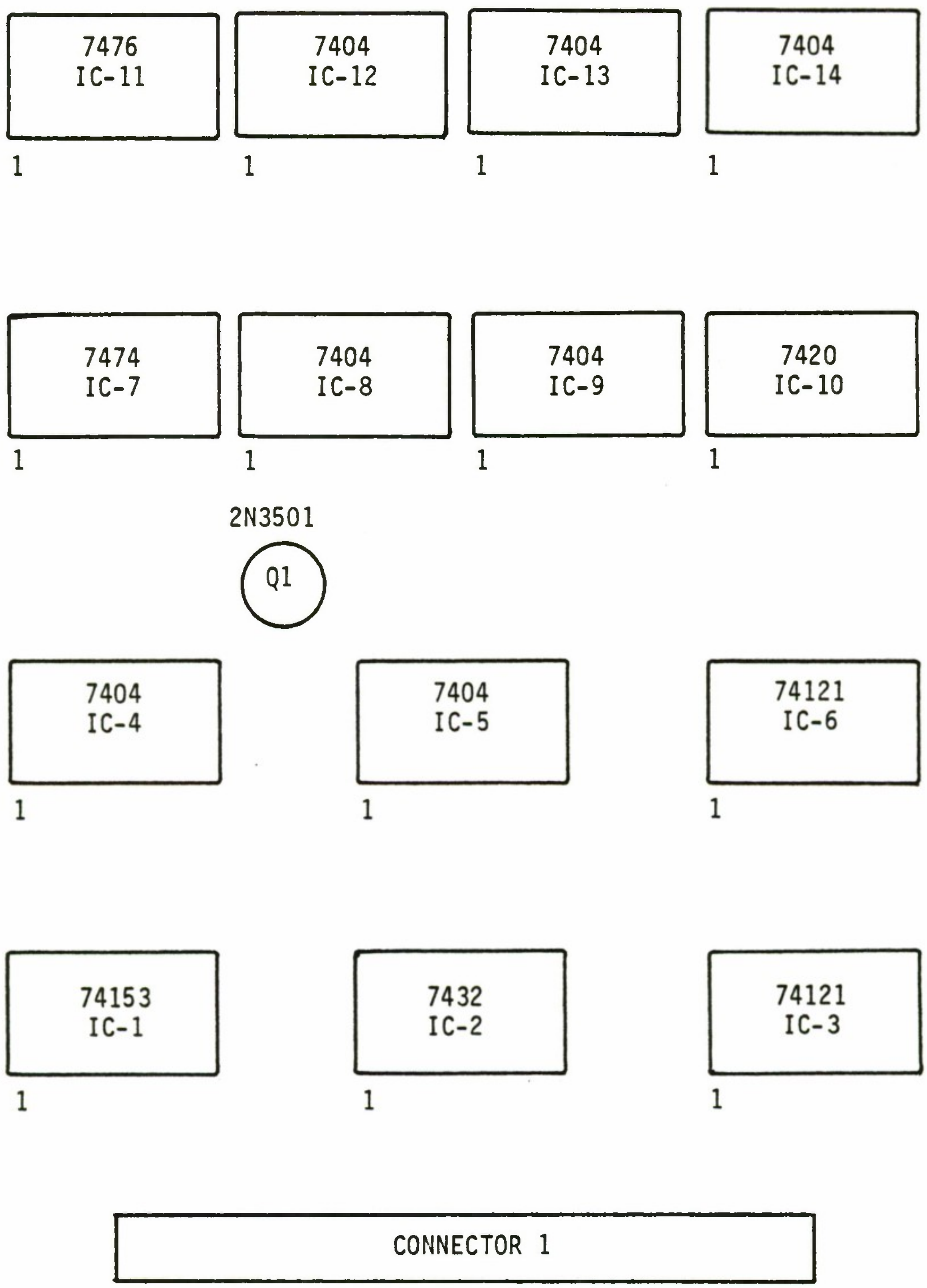
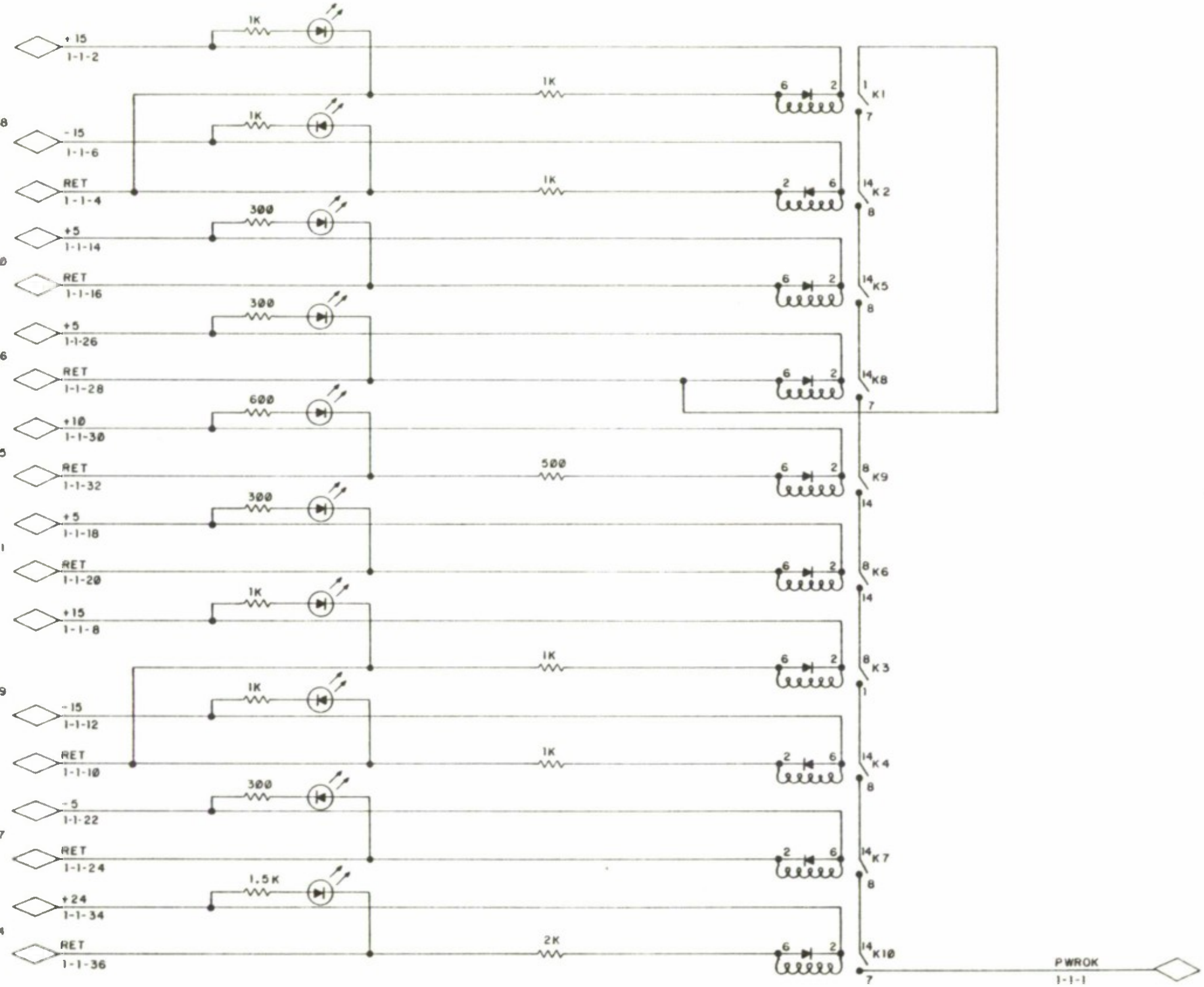



Figure 16. ADC Prestart Board Component Layout




ALL RELAYS PRMA1A05C
INTERNAL DIODE PINS 2 AND 6

Figure 17 - ADC Protect Circuit Auxiliary Board 4

reed relay. Each Power supply voltage (through a resistor if needed) is applied across pins 2 and 6 of its respective relay. Due to a protective diode internal to the relay, the more positive terminal of the power supply must be applied to pin 2 of the relay. The switched contacts of all ten relays are connected in series to provide output line, PWROK, a path to ground only if all power supplies are operational.

c. Light-Emitting-Diodes

Each DAU power supply in addition to driving a relay, also powers its own LED indicator lamp located on auxiliary board 4 so as to be visible from the top of the DAU. Current limiting resistors protect the LED's from overcurrent. In the event that any power supply is non-operational quick inspection will indicate the faulty power supply by a light-out condition.

d. PWROK Output Signal

With all DAU power supplies operational, PWROK, edge connector pin 1-1-1 provides a path to ground through the series connection of each relay. PWROK is connected to both High Speed ADC boards (Figure 5) and both Low Speed ADC boards (Figure 8) and to the front panel indicator LED. Each ADC board has an additional PRMA 105C relay to switch the analog signal input to the sample-and-hold modules. In the event that any DAU power supply is non-operational, PWROK will remove the ground path to the ADC board relays, thus removing analog signal to the S/H modules. Additionally, the front panel LED will be switched off indicating a non-operational DAU.

e. Component Layout

Figure 18 shows the major component layout for the ADC Protect Circuit.

6. <u>Buffer Memory Input Selector Circuit Board</u>

a. Introduction

The DAU contains two Buffer Memory Input Selector Circuit boards, DAU board 2Ø and DAU board 4, to allow proper routing of channel 1 and channel 2 data respectively, to the Buffer Memory Circuit boards (Section II.C.7.). This circuit, shown in Figure 19, makes possible the parallel loading of both channels of buffer memory with high speed ADC data, low speed ADC data or INTERDATA 7/32 diagnostic software data depending on the address code supplied to the input multiplexor register.

b. Input Multiplexer Register

Compatible with the 12 bit wide word length of the buffer memories, the input selector circuit utilizes six 74153 dual one of four multiplexer chips (IC-4 through IC-9) to provide 12 bits of input data per channel. Multiplexer address lines ASEL and BSEL, brought in through edge connector pins 4/20-1-1Ø and 4/2Ø-1-12 from the control (1 of 2) circuit board (Section II.C.12.) determines if the input is selected from high speed ADC data, low speed ADC data or from the latched INTERDATA 7/32 Diagnostic input port. The input data lines from the high speed ADC boards, in order to fill a field of 12 from a field of 8, have the low four significant bits wire wrapped to ground (i.e., the work is left justified). The address lines ASEL and BSEL, for multiplexer selection, are coded as shown in Table III. ASEL and BSEL are generated by inverting ADC-HI and ADC-LO from the Control Board (1 of 2) at the Auxiliary Board 2 shown in Figure 3Ø. Note that ADC-HI and ADC-LO signals (never selected simultaneously) have been wired as a null condition on the multiplexer register.

c. Diagnostic Input Data Port

To provide for DAU problem correction diagnostics, the input selector circuit was designed with an input port to facilitate the loading of software generated diagnostic data. When binary code three (i.e., 11) is selected, diagnositc data from the INTERDATA 7/32 via the ULI interface can be loaded, one channel at a time, into the buffer memory. Diagnostic data arriving at the DAU via the 16 bit data out (DOT) bus from the ULI, is first latched onto the Buffer Memory Input Selector boards into three 74175 quad latch chips, IC-1 through IC-3. The diagnostic data words (12 bits left justified in a field of 16) must be first latched onto the channel 1 board, and then the corresponding part of a complex data point next latched onto the channel 2 board. Subsequent to the second word being latched, both channels of data are written into buffer memory in parallel. Control for

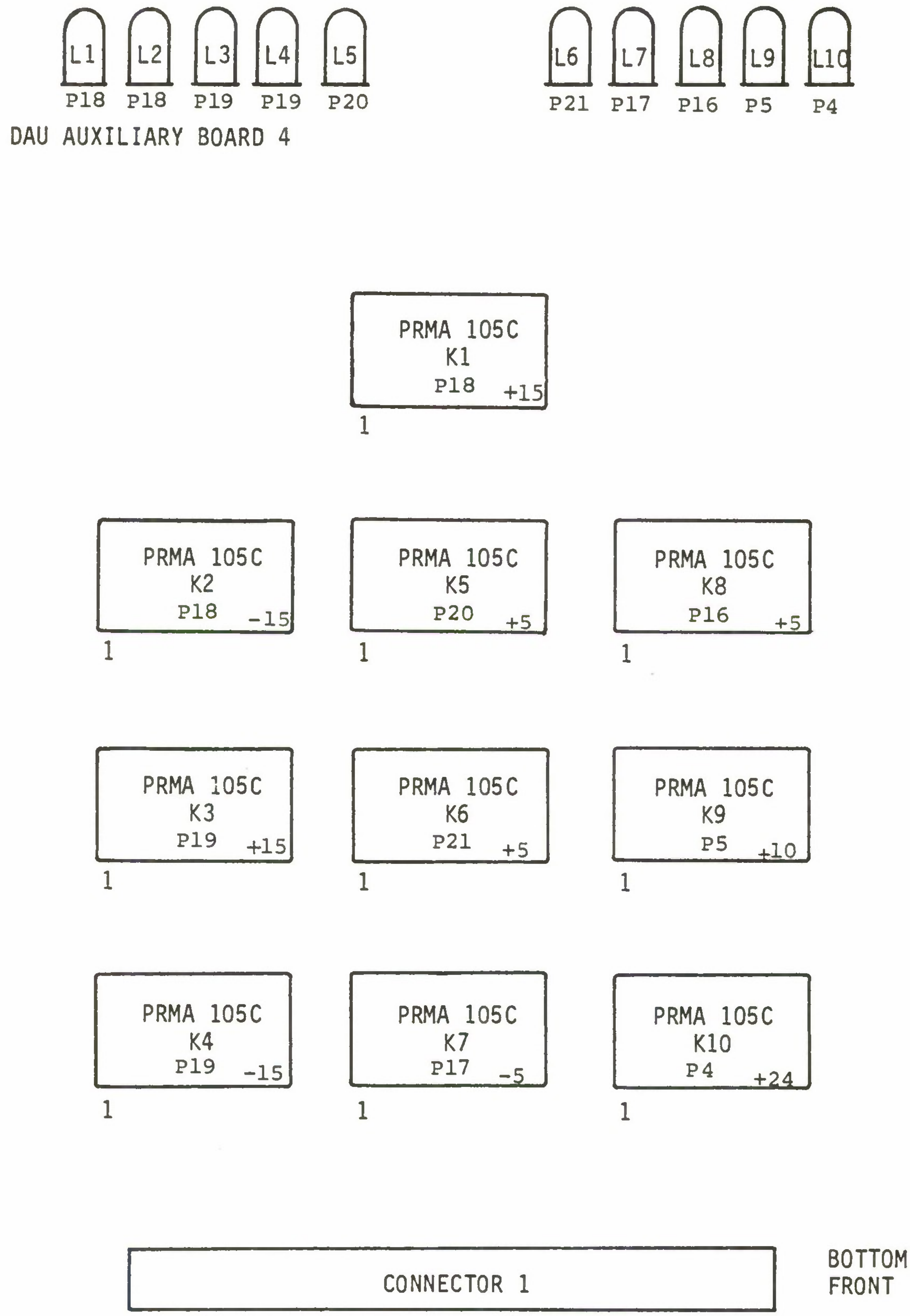



Figure 18. ADC Protect Circuit Component Layout

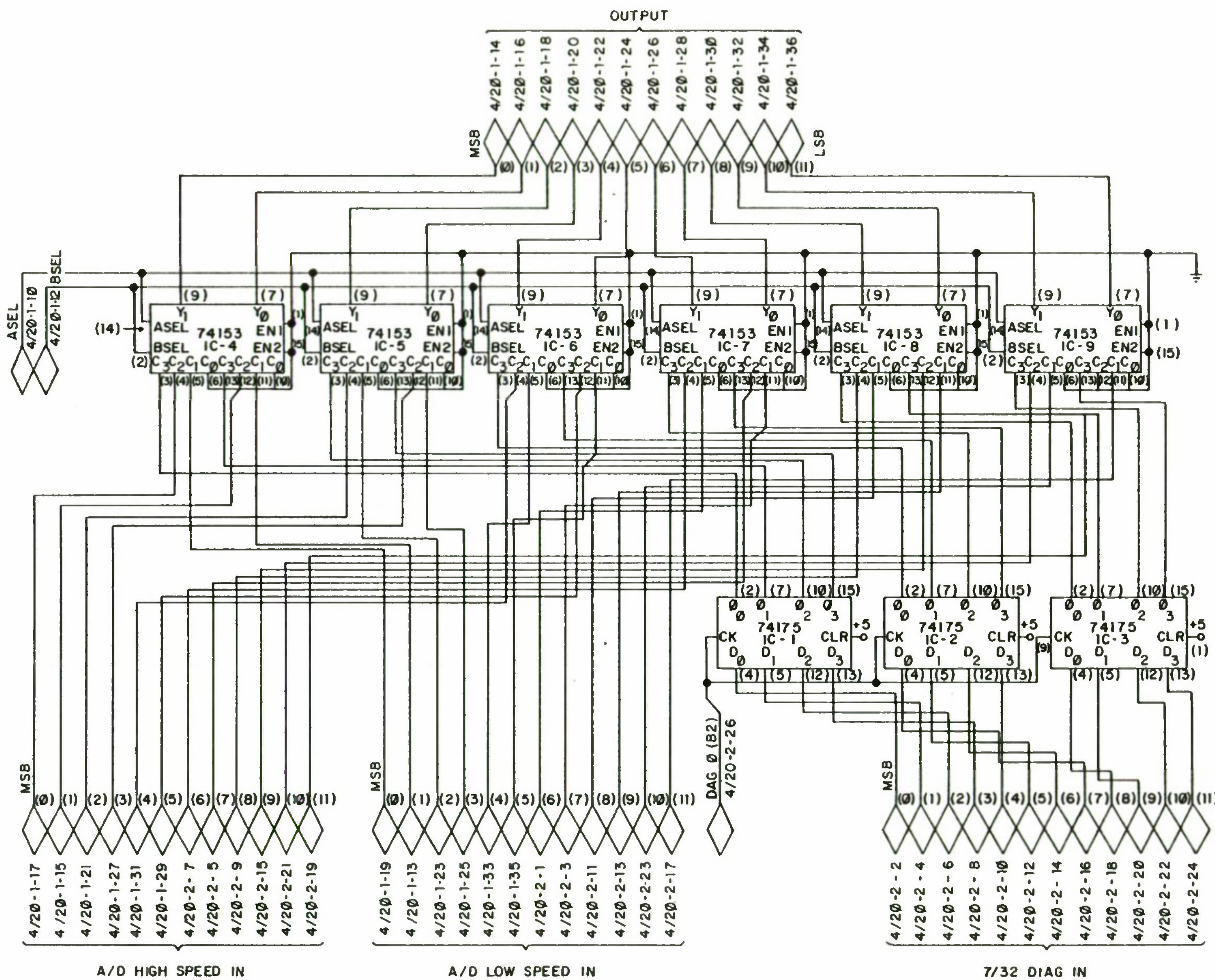



Figure 19 - Buffer Memory Input Selector Circuit

TABLE III - BUFFER MEMORY INPUT SELECTOR CODES

| Control Board (1 of 2) | | Input Selector | | Input Selected |
|---|---|---|---|---|
| ADC-LO | ADC-HI | $\overline{BSEL}$ | $\overline{ASEL}$ | |
| 1 | 1 | 0 | 0 | Null-wired to ground |
| 1 | 0 | 0 | 1 | Low Speed ADC data |
| 0 | 1 | 1 | 0 | High Speed ADC data |
| 0 | 0 | 1 | 1 | INTERDATA Diagnostic data |

this sequence is accomplished by the Buffer Memory Timing circuit (Section II.C.8.). Also generated by the Buffer Memory Timing Circuit are the DAGØ B1 and DAGØ B2 signals used to clock respectively the channel 1 and channel 2 input selector diagnostic latches through edge connector pins 2Ø-2-26 and 4-2-26. This entire diagnostic loading operation can be performed manually using the DAU Test Panel as discussed in Section II.F.2.

d. Buffer Memory Input Circuit Timing Diagram

The timing sequence associated with this circuit is shown in Figure 2Ø. It is shown for dual channel operation to put into perspective the loading of diagnostic data. Reference should be made to Buffer Memory Timing Circuit (II.C.8.). Table IV shows associated signals.

e. Voltage Requirements

All power for boards 4 and 2Ø is supplied by the plus 5 volt main logic power supply located in the lower rear of equipment rack 16.

f. Buffer Memory Input Selector Component Layout

Major component layout for this circuit is shown in Figure 21.

7. <u>Buffer Memory Circuit Board</u>

a. Introduction

DAU board 18 and board 6 each contain 2Ø48 12 bit words of random access memory (RAM) designed as data buffer storage for channel 1 and channel 2 respectively. This buffer

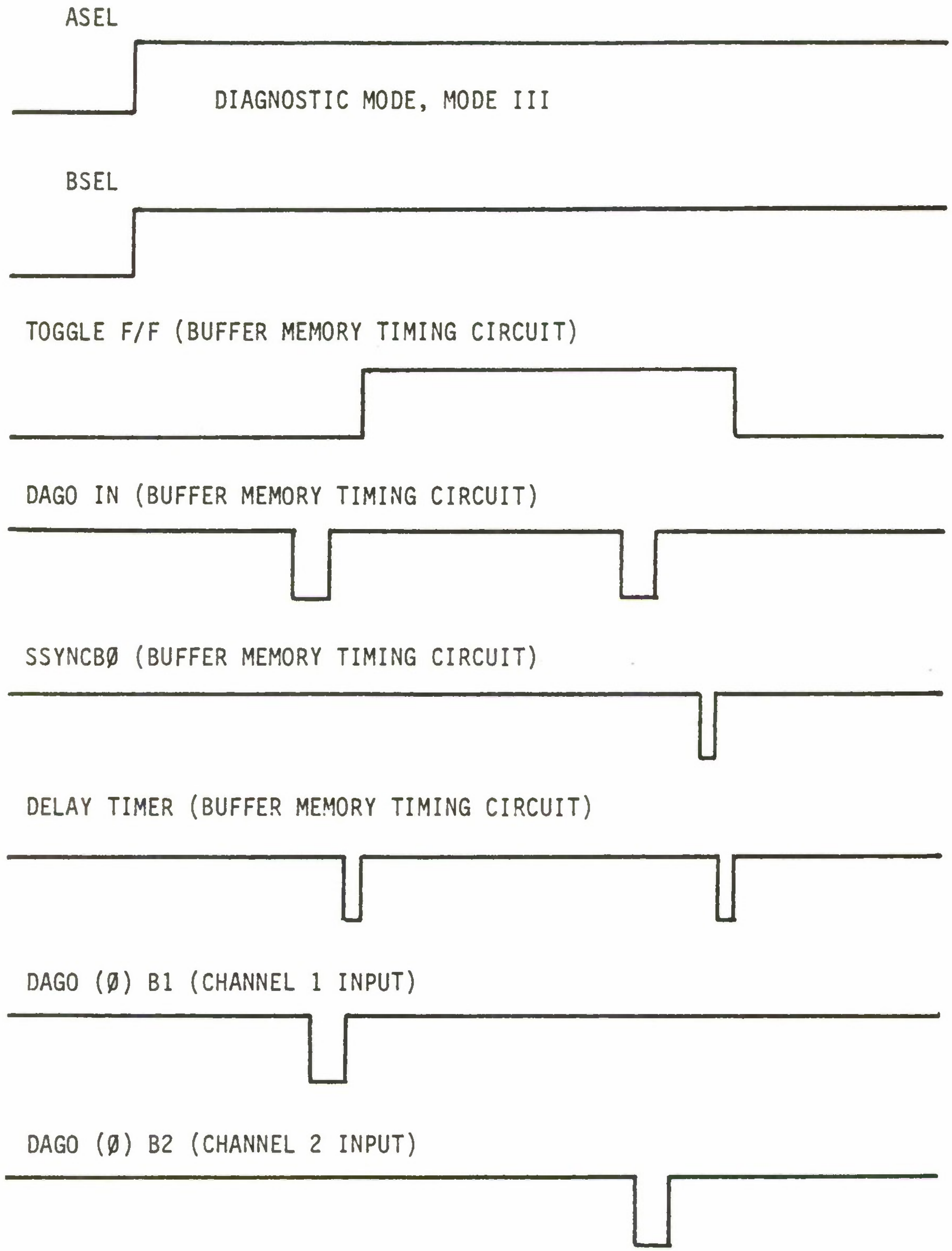



Figure 20. Buffer Memory Input Selector Timing Diagram

TABLE IV. BUFFER MEMORY INPUT SELECTOR SIGNALS AND BUFFER MEMORY SIGNALS

| Signal Name | Source | Destination | Purpose | Ref (Page) |
|---|---|---|---|---|
| ASEL | Inverter Bd | Input Selector Bds | Select Input Data Source | Sec II.C.6.b. |
| BSEL | Inverter Bd | Input Selector Bds | Select Input Data Source | Sec II.C.6.b. |
| DAGØ | INTERDATA 7/32 ULI | Control Board (1 of 2) | Synchronize Data Transfer from 7/32 to DAU | Sec II.C.13.c. |
| TOGGLE F/F | Buff Mem Timing Bd | Buff Mem Timing Bd | Generate DAGOB1(Ø) and DAGØB2(Ø) | Sec II.C.8.c. |
| DAGØB1(Ø) | Buff Mem Timing Bd | Input Selector Bd Chn1 | Clock in 7/32 data | Sec II.C.8.d. |
| DAGØB2(Ø) | Buff Mem Timing Bd | Input Selector Bd Chn2 | Clock in 7/32 data | Sec II.C.8.d. |
| $\overline{\text{WE}}$ | Buff Mem Timing Bd | Buff Mem Bds | Write Input Data to RAM | Sec II.C.8.b. |
| CS/$\overline{\text{CS}}$ | Driver Bd | Buff Mem Bds | Enable RAM Chips | Sec II.C.9.b |
| SSYNCBØ | Buff Mem Timing Bd | Control Board (2 of 2) Buff Mem Output Sel, Control Board (1 of 1) | Indicates End of Cycle | Sec II.C.8.b. |

NOTE: See Table VI for related signals.

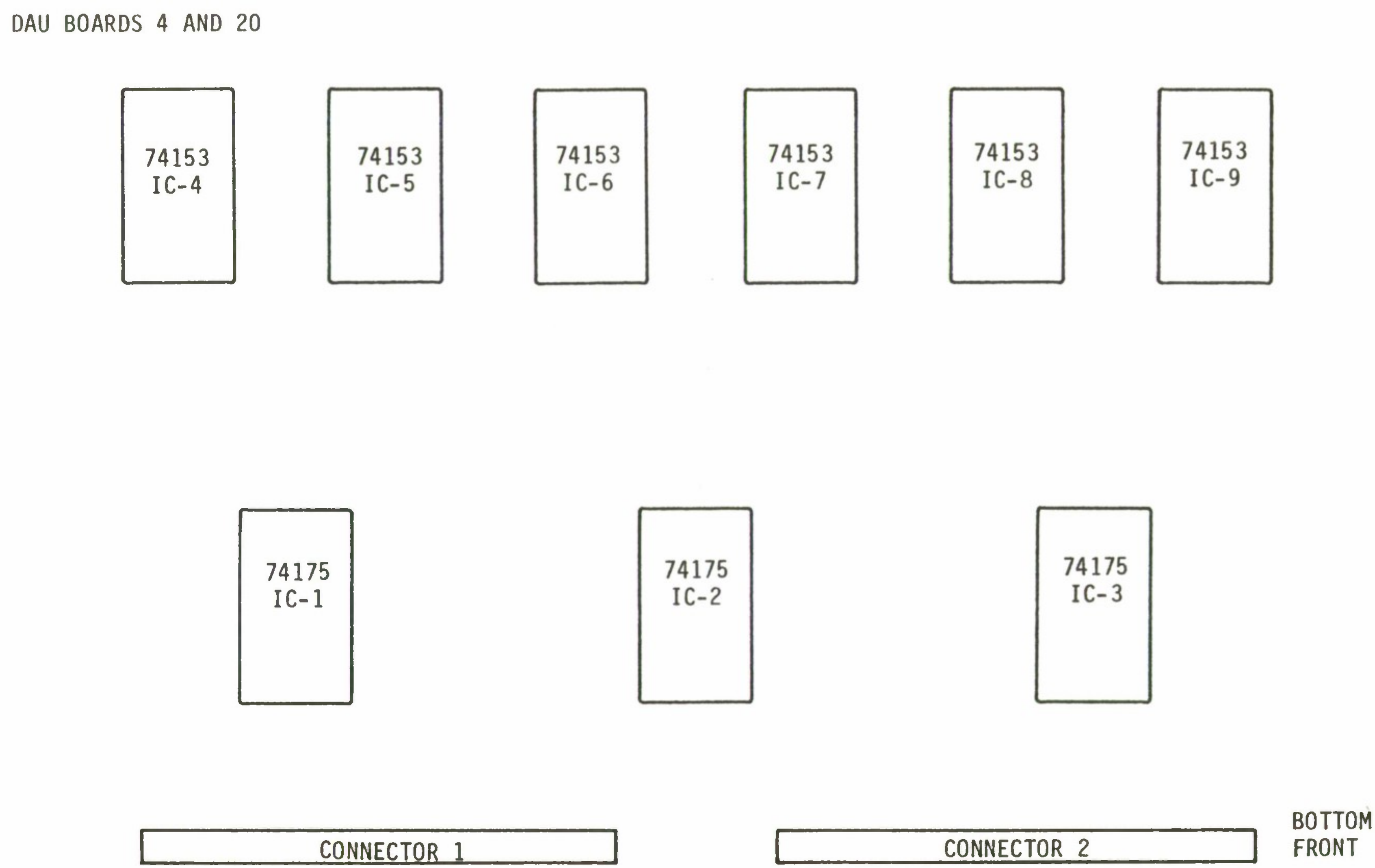



Figure 21. Buffer Memory Input Selector Component Layout

RAM is necessary to facilitate data acquisition at high speed rates above the direct memory access (DMA) data transfer rates possible with either the INTERDATA 7/32 of the AP-120B array processor and also to allow all transfers to be DMA with minimum processor overhead time. See Figure 22.

b. FAIRCHILD 93415 RAM

The Buffer Memory Circuit is designed around the FAIRCHILD 93415 1024 x 1 bipolar RAM chips, chosen for their fast (35 nanosecond) access time as required for this application. These chips have open collector outputs, 10 bit addressing, a chip select (CS) line and a write enable ($\overline{WE}$) line. Open collector outputs allow outputs to be tied together on the output data bus provided no two chips tied in common will be addressed simultaneously.

c. Block Partition Design

Arranging 12 93415 chips in parallel provides a 1024 x 12 block of RAM containing 1024 12 bit words (=12288 bits) of storage capacity. Two such blocks of RAM make up each channel of buffer memory. The $\overline{WE}$ input and address lines zero through nine, driven by 7438 open collector bus driver chips on auxiliary board 1 (Section II.C.9.), are paralled to all 24 of the 93415 chips on each Buffer Memory Circuit board (i.e., 48 chips). External pull up resistors for the address lines are located on the buffer memory boards. There are 12 data input lines and 12 data output lines for each buffer memory channel. Each Buffer Memory Board is

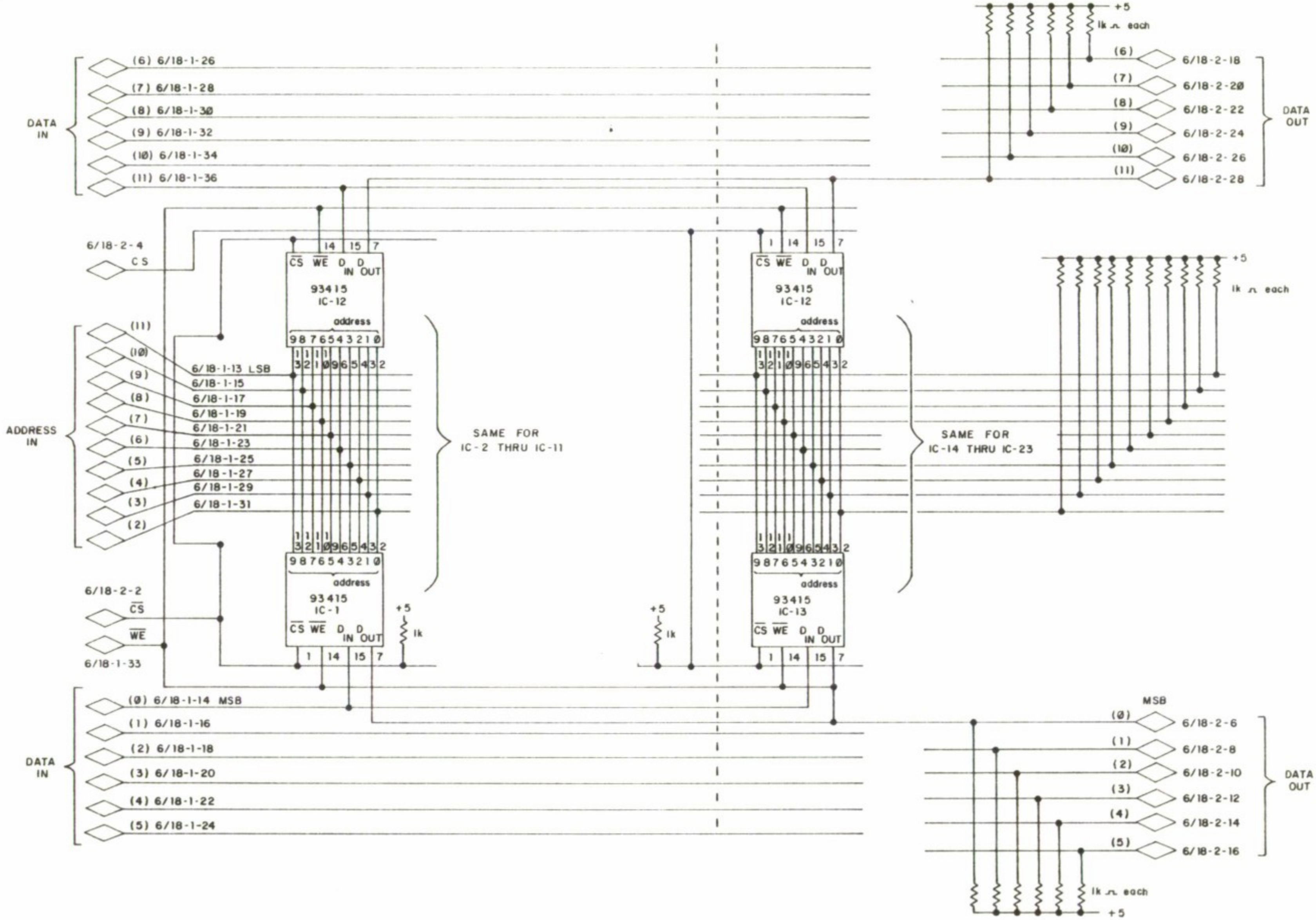



Figure 22 - Buffer Memory Circuit

made up of two 1K work blocks of memory with parallel input and output data between the 1K blocks. For example, data input bit zero is sent to IC-1 and IC-13, while data output bit zero comes from IC-1 and IC-13. In this fashion IC-1 through IC-12 represents bits "Ø" through "11" for addresses Ø through 1Ø23, and IC-13 through IC-24 represents bits "Ø" through "11" for addresses 1Ø24 through 2Ø47.

d. Buffer Memory Addressing Scheme

Eleven bits of address, bits "1" through "11", are generated on the Control Board (2 of 2), Section II.C.13., in the address register. Address input lines "2" through "11" paralleled to 93415 inputs AØ through A9, provide address locations Ø through 1Ø23. Address bit "1" from the Control Board (2 of 2) is separated into a CS and $\overline{\text{CS}}$ signal on auxiliary board 1, to be used for block control in the Buffer Memory Circuit. Hence the state of CS and $\overline{\text{CS}}$, edge connector pins 6/18-2-4 and 6/18-2-2 respectively, determines whether memory block Ø through 1Ø23 through 2Ø47 is being addressed.

e. Input Data Bus

Input data to be stored in the buffer memories is selected as appropriate by the Buffer Memory Input Selector Circuit (Section II.C.6.) and made available on the input data bus. This data must be available during the correct time period to allow it to be written into memory.

f. Write Enable, $\overline{\text{WE}}$

A 35 nanosecond active low $\overline{\text{WE}}$ signal is generated on the Buffer Memory Timing Circuit Board (Section II.C.8.) and pulsed each time a set of input data is to be stored in parallel into channel 1 and channel 2 buffer memory. During the time of this active low pulse input data on the input data bus will be stored in RAM at the location pointed to by the address bus lines and CS/$\overline{CS}$. At all other times $\overline{WE}$ is high and output data is read from the buffer memory location pointed to by the address bus and CS/$\overline{CS}$. Note that data stored at a particular address location by $\overline{WE}$ can be immediately read out onto the output data bus provided the address lines are not changed immediately after the $\overline{WE}$ pulse. This fact is utilized in future design modifications (Section V).

g. Output Data Bus

Output data is available on the output data bus, to be latched onto the Buffer Memory Output Selector board (Section II.C.11.) when appropriate, at all times that $\overline{WE}$ is high. Thus the output data bus is constantly stabilizing to the data stored at the location pointed to by the address lines and CS/$\overline{CS}$.

h. Buffer Memory Timing Diagram

The timing associated with the buffer memory circuits for both the write and the read mode is shown in Figure 23.

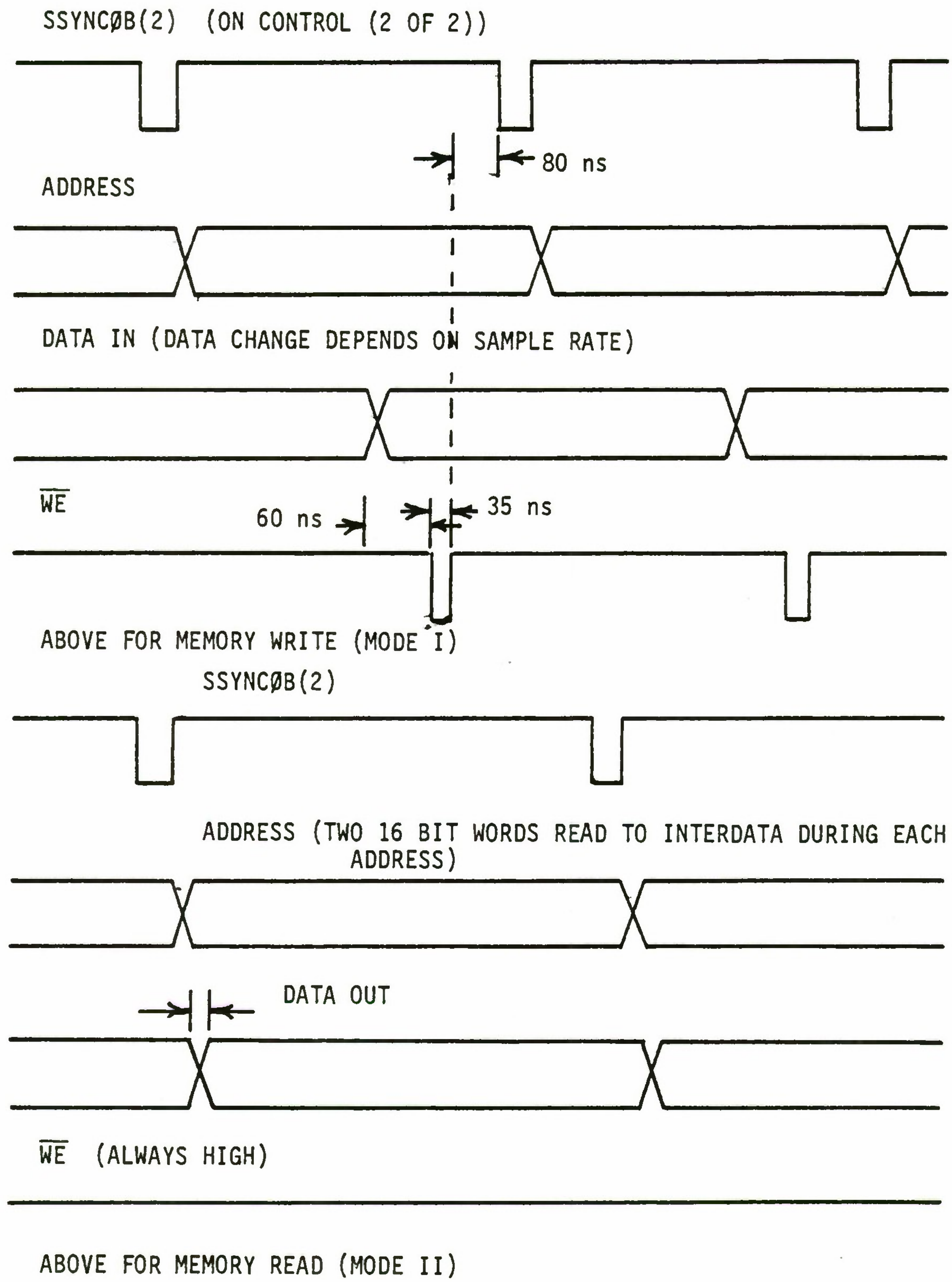



Figure 23. Buffer Memory Circuit Timing Diagram

i. Voltage Requirements

Because bipolar RAM chips are heavy power consumers, the two buffer memory boards consume the major portion of the main logic power supply located in the lower rear section of equipment rack 16.

j. Component Layout

Figure 24 shows the major component layout for this circuit.

8. Buffer Memory Timing Circuit

a. Introduction

The Buffer Memory Timing Circuit, Figure 25, located on DAU board 16 performs several important functions pertinant to DAU operation. This circuit coordinates interaction ("handshaking") between the A/D (Section II.C.2. and 3.), the INTERDATA 7/32, the Buffer Memory Input Selector Circuit (Section II.C.6.), the Buffer Memory Circuit (Section II.C.7.), the Buffer Memory Output Selector Circuit (Section II.C.11.), the Control Board (1 of 2) (Section II.C.12.) and the Control Board (2 of 2) (Section II.C.13.). To facilitate the understanding of this circuit, three different but distinct modes of DAU operation will be discussed. Listed in Table V is each mode and the appropriate associated signals generated for both internal and/or external use. Mode I operation is used during data acquisition to store A/D converted data into buffer memory. Mode II operation is used to DMA transfer the acquired data from buffer memory to the

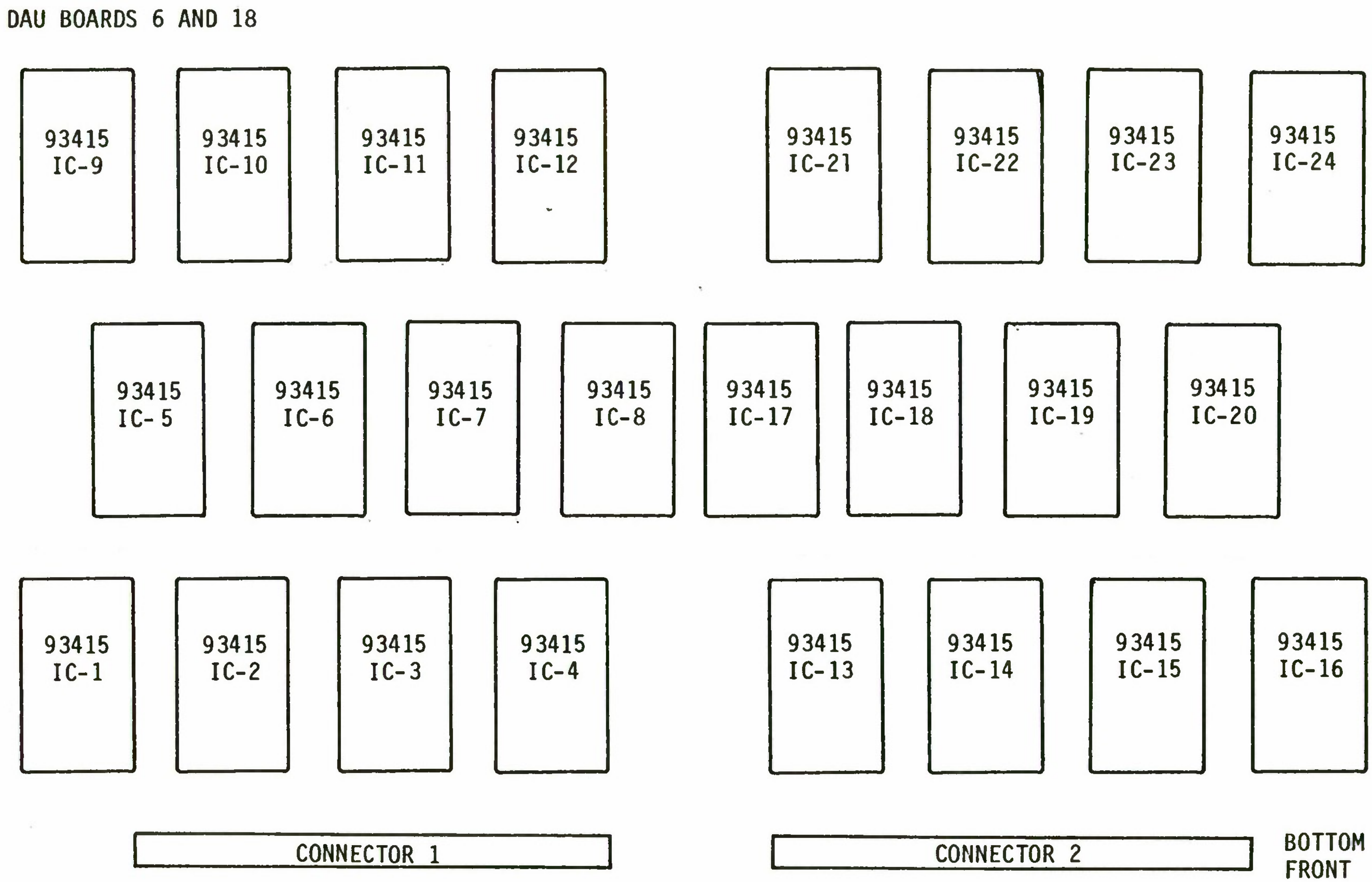



Figure 24. Buffer Memory Circuit Component Layout

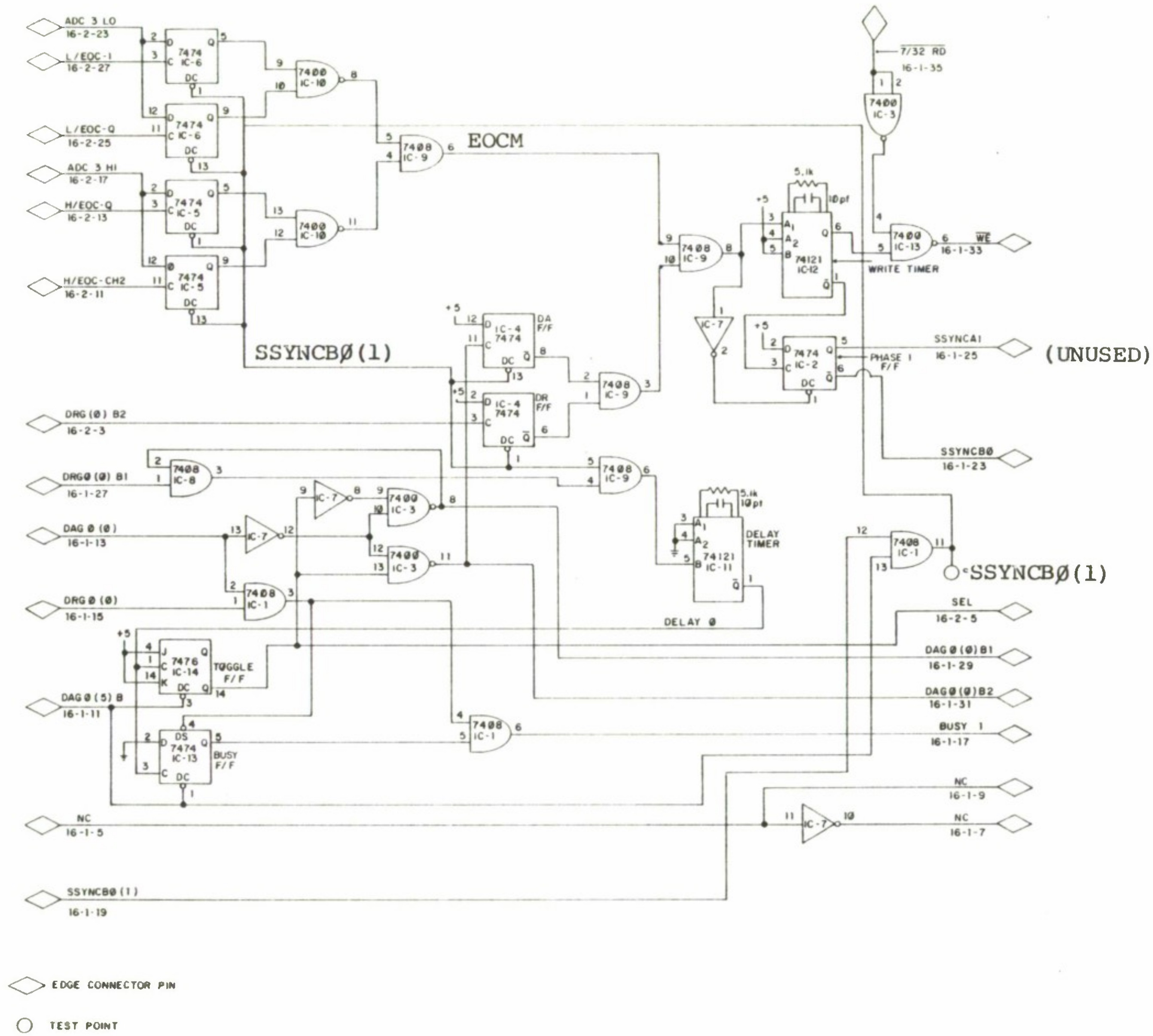



Figure 25 - Buffer Memory Timing Circuit

TABLE V - DAU MODES AND ASSOCIATED SIGNALS

| Mode | Signal Generated for Internal use | Signal Generated for Internal and/ or External use |
|---|---|---|
| I. Data acquisition and storage in buffer memory | EOCM<br>7/32 RD | $\overline{\text{WE}}$<br>SSYNCBØ<br>SSYNCB1(Ø) |
| II. DMA transfer of stored data to INTERDATA 7/32 | DR F/F<br>TOGGLE F/F<br>BUSY F/F<br>DELAY Ø | SSYNCBØ<br>BUSY 1 |
| III. Diagnostic data loaded to buffer memory | DA F/F<br>TOGGLE F/F<br>BUSY F/F<br>DELAY Ø | SSYNCBØ<br>DAGØ(Ø)B1<br>DAGØ(Ø)B2<br>BUSY 1 |

INTERDATA 7/32. Mode III operation is used to load diagnostic data into the buffer memory.

b. Mode 1 Operation

(1) <u>Generation of $\overline{WE}$</u>. Write enable ($\overline{WE}$) is a 35 nanosecond, active low pulse generated precisely at the correct time to "write" both channels of A/D converted data into the buffer memories in parallel. Referring to Figure 25, four 7474 D flip-flops, IC-5 and IC-6, are used to bring into coincidence the active A/D converter end-of-convert (EOC) signals, be they the low speed channel 1 and channel 2 EOC signals or the high speed channel 1 and channel 2 EOC signals or the high speed channel 1 and channel 2 EOC signals. This technique, used to compensate for inherent differences between conversion times for the ADC boards, waits until the slower of the two EOC signals clocks Q high in that flip-flop at which time the output of the assoicated NAND gate, pin 8 or pin 11 on IC-1Ø, goes low. The AND gate characteristics operate on active low signals as an OR function. Utilizing this idea the active low signal from either of the coincidence producing NAND gates, is OR'ed through the 74Ø8 AND gate on IC-9 to produce the end-of-convert master (EOCM) signal at pin 6. The active low EOCM is then OR'ed through a second 74Ø8 gate on IC-9 to bring pin 8 low. That high-to-low transition applied to pin 3 of the WRITE TIMER, a 74121 monostable multivibrator, IC-12 triggers a 35 nanosecond positive pulse at the Q output, pin 6. In mode I the

7/32 RD input on edge connector pin 16-1-35 is low, which is inverted by the 74ØØ NAND gate on IC-3 to apply a high level to pin 4 of IC-3, a second 74ØØ gate. The WRITE TIMER output pulse is applied to pin 5 of that same 74ØØ gate to generate the $\overline{WE}$ active low pulse out on pin 6, which leaves the board via edge connector pin 16-1-33.

Note that EOCM can be disabled at the D flip-flops if the ADC3-LO or ADC3-HI signal (edge connector pins 16-2-23 and 16-2-17), generated by the ADC Prestart Circuit (Section II.C.4.) is low. It is this method that allows the ADC Prestart Circuit to operate the A/D converters for 2 milliseconds at 25Ø KHz for the prestart period, without writing that invalid data into the buffer memories.

(2) Generation of SSYNCBØ. The slave sync pulse (SSYNCBØ), probably the most important pulse in the DAU, is generated at the completion of each cycle for the three modes. This pulse is used to clear various asynchronous logic gates in the DAU and eventually generate the interface logic to "handshake" with the INTERDATA 7/32. In Mode I SSYNCBØ is the only important pulse internal to the DAU operation.

In mode I the 7474 D flip-flop on IC-2 (SSYNC F/F) is direct cleared by EOCM via the 74Ø8 gate IC-9 and the 74Ø4 inverter pins 1 and 2 of IC-7. When EOCM goes low at the coincidence of the EOC's for the operational A/D converters, the inverter brings the direct clear (DC) pin 1 of IC-2 high to enable the SSYNC F/F. When the WRITE TIMER

IC-12 pulses its $\overline{Q}$ output pin 1, tied to the clock input of SSYNC F/F pin 3, latches SSYNCBØ on the trailing edge to bring the $\overline{Q}$ output, pin 6, low. The SSYNCBØ is output to edge connector 16-1-23 and sent to the auxiliary board 2 (Section II.C.1Ø.) where it propagates through six 74Ø4 inverters to provide 6Ø nanoseconds of delay, and the brought back as SSYNCB1(Ø) on edge connector 16-1-19. SSYNCB1(Ø) is OR'ed through the 74Ø8 gate to pin 11 of IC-1 which is tied back around the board as feedback to direct clear the EOC flip-flops, IC-5 and IC-6, plus the DA F/F and the DR F/F, and eventually trigger the DELAY TIMER, IC-11. The DA F/F, DR F/F and DELAY TIMER are discussed in conjunction with modes II and III. When the SSYNCB1(Ø) low level direct clears the EOC flip-flops, they return their outputs to low which propagates through to bring EOCM high. EOCM high, inverted through the 74Ø4 gate IC-7 then direct clears the SSYNC F/F which brings SSYNCBØ high. Thus the SSYNCBØ active low level is terminated by "itself" through the feedback loop to create approximately a 12Ø nanosecond pulse. At the trailing edge of the SSYNCBØ pulse, the EOC flip-flops have been reset to await the arrival of the next cycle of EOC signals and continue the writing of data to buffer memory.

c. Mode II Operation

(1) Generation of SSYNCBØ. Generation of SSYNCBØ for Mode II operation is similar to that described in Section II.C.8.b.(2) for Mode I operation, utilizing the WRITE TIMER

and the SSYNC F/F with feedback for pulse termination. However, in Mode II EOCM is not active and hence remains high, while the data request flip-flop (DA F/F), when clocked by input signal DRGØ(Ø)B2 from edge connector pin 16-2-3, provides an active low level to propagate through two 74Ø8 gates on IC-9, trigger the WRITE TIMER and then the SSYNC F/F. The DR F/F is direct cleared by SSYNCBØ(1) which indirectly terminates SSYNCBØ and leaves the DR F/F reset for the next DRGO(Ø)B1. Note the SSYNCBØ pulse in Mode II occurs as the termination of a complete "read" cycle, but a complete cycle in this sense means two read operations, one for the channel 1 data and another for the channel 2 data. This concept is further discussed in the following section.

(2) Generation of DRGO(Ø) B1 and DRGØ(Ø)B2. In order to adequately discuss the complete operation of Mode II then DRGØ(Ø)B1 and DRGØ(Ø)B2 signals generated on auxiliary board 1 (Section II.C.9.) must be understood. The DRGØ(Ø)B1 and DRGØ(Ø)B2 signals are simply the creation of two pulses from one, accomplished by four NAND gated on IC-1 of auxiliary board 1, Figure 28. The data available, gated (DRGØ) signal entering on edge connector pin 12-1-6, is an interface active low pulse, generated by the INTERDATA 7/32 ULI board, in conjunction with a DMA operation. Data words "read" out of the DAU to the ULI must be done in 16 bit words or less, which requires that two words must be read from the DAU for each complex data point stored (i.e. each pair of

data words in channel 1 and channel 2). Because the DAU address bus during any mode, can only be controlled by the address register on the Control Board (2 of 2), Section II.C. 13., Mode II operation is facilitated by the generation of DRGØ(Ø)B1 and DRGØ(Ø)B2.

The TOGGLE F/F input on edge connector pin 12-1-8 of the auxiliary board 1, generated on the Buffer Memory Timing board, determines whether an incoming DRGØ(Ø) pulse on pin 12-1-6 will generate a DRGØ(Ø)B1 pulse or a DRGØ(Ø)B2 pulse. When TOGGLE F/F is low, pin 12 of the 74ØØ NAND gate, IC-1, is low assuring that DRGØ(Ø)B2 stays high. Pin 1Ø of the 74ØØ NAND gate, IC-1, will be high after TOGGLE F/F was inverted through pin 5 to pin 6 of IC-1. When an active low DRGØ(Ø) pulse arrives it is first inverted by pin 1 to pin 3 of IC-1, which applies a high to pin 9 and pin 12 of IC-1, which generates DRGØ(Ø)B1 and does nothing to DRGØ(Ø)B2. When the TOGGLE F/F input is high the opposite condition exists to create the DRGØ(Ø)B2 pulse for the DRGØ(Ø) input. Keeping in mind how the DRGØ(Ø)B1 and DRGØ(Ø) B2 pulses are generated, a complete read out cycle of Mode II operation can be discussed.

Mode II operation is started when input DAGØ(5)B on edge connector 16-1-11 of the Buffer Memory Timing board pulses low. DAGØ(5)B direct clears both the TOGGLE F/F a 7476 J-K flip-flop, IC-14, and the BUSY F/F, a 7474 D flip-flop, IC-13, plus DAGØ(5)B being OR'ed through a 74Ø8 gate pin 13 of IC-1, direct clears everything in the SSYNCB1(Ø) feedback loop and fires the DELAY TIMER, IC-11, which clocks TOGGLE F/F into the low state at $\overline{Q}$, pin 14 (TOGGLE F/F is a J-K flip-flop set to toggle). The TOGGLE F/F set low is sent via the SEL output pin 16-2-5 to auxiliary board 1 which causes the first DRGØ(Ø) pulse coming from the INTERDATA 7/32 ULI board to generate a DRGØ(Ø)B1 pulse. The SEL output also supplies the Buffer Memory Output Selector board (Section II.C.11.) to select either channel 1 data (SEL low) or channel 2 data (SEL high) for output to the data input bus (DIN lines).

When the DAU is ready to provide data to the INTERDATA 7.32, the Control Board (1 of 2) puts output line SATNO, low. When the INTERDATA 7/32 is ready to accept a word of DMA data it sends a DRGO pulse to the DAU which is passed as DRGO (Ø) to auxiliary board 1 to generate DRGØ(Ø)B1 and also to the Buffer Memory Timing board, pin 16-1-15. DRGØ(Ø) is OR'ed through 74Ø8 gate pin 1, IC-1 where it direct sets the BUSY F/F, pin 4, IC-13, and holds BUSY 1 low via 74Ø8 gate pin 4, IC-1. At the trailing edge of DRGØ(Ø), both pins 4 and 5 of the 74Ø8 gate, IC-1, are high which asserts active low BUSY Ø and returns SATNO high on the Control Board (1 of 2). SATNO high indicates that the end of the first read has occurred. Simultaneous to the action at DRGØ(Ø), DRGØ(Ø)B1 was OR'ed through 74Ø8 gate, pin 1, IC-8. On its leading edge, DRGØ(Ø)B1 clocks pin 1 of the TOGGLE F/F to change its state for the second read of the cycle, and it also clocks the BUSY F/F low, on its trailing edge, removing BUSY 1 and reasserting SATNO low, thus calling for the INTERDATA 7/32 to take the next data word. In this manner the DELAY TIMER provides clocking for DMA transfers via the Extended Selector Channel (ESELCH) in the INTERDATA 7/32 /Ref. 9 /. If the DMA transfer were to be driven at the buffer memory rate capability, any other DMA in progress on the other ESELCH and all CPU activity would be locked out due to every INTERDATA 7/32 memory cycle being allocated to the DAU.

The second hald of the read cycle, when initiated by the INTERDATA with another DRGØ pulse, sets up BUSY 1 just as before, but now sends in DRGØ(Ø)B2, pin 16-2-3, which latches the DR F/F low, IC-4, and OR's through to trigger the WRITE TIMER and SSYNCBØ as discussed in Section II.C.8.c.(1). This action does not initiate $\overline{\mathrm{WE}}$ due to the state of 7/32 RD, but it does clear all flip-flops via SSYNCB(Ø)1 and OR'ed through 74Ø8 gate, pin 5, IC-9, triggers the DELAY TIMER to operate as described above. Also SSYNCB(Ø)2 clocks the address and WC registers on Control Board (2 of 2) to the next value for a new cycle. Note that the first pair of words read by the INTERDATA in Mode II operation are ignored for reasons discussed in Section II.C.11.

d. Mode III Operation

(1) <u>Generation of SSYNCBØ</u>. In Mode III operation,

SSYNCBØ is generated exactly as discussed in Mode II operation except that the DA F/F IC-4 is latching the low level that initiates the chain of events (see Section II.C.8.c.(1).). During this mode diagnostic input data is being latched into the Buffer Memory Input Selector boards channels 1 and 2, to be written to buffer memory in parallel during the $\overline{\text{WE}}$ pulse.

(2) <u>Generation of DAGØ(Ø)B1 and DAGØ(Ø)B2</u>. Just as the data out port to the INTERDATA 7/32 is only 16 bits, the data in port (DOT lines) in only 16 lines, which necessitates the loading of two diagnostic words to represent one complex data point. For this reason, there exists a great deal of similarity between the diagnostic load cycle of Mode III and the read cycle of Mode II. For the Mode III case the INTERDATA 7/32 responds to SATNO with data available, gated (DAGØ). The DAGØ pulse is routed through the Control Board (2 of 2) to be passed on as DAGØ(Ø). Again DAGØ(Ø) is split into DAGØ(Ø)B1 and DAGØ(Ø)B2 pulses that function identically on the Buffer Memory Timing board to the DRGØ(Ø)B1 and DRGØ(Ø)B2 (see Generation of DRGØ(Ø)B1 and DRGØ(Ø)B2). Additionally, DAGØ(Ø)B1 and DAGØ(Ø)B2 are sent to the Buffer Memory Input Selector boards to latch diagnostic data at the appropriate time. In this mode the 7/32 RD input enables $\overline{\text{WE}}$ to allow the buffer memories to be written into. BUSY 1 serves the same purpose in Mode III as in Mode II.

e. Buffer Memory Timing Circuit Timing Diagram

The timing diagram for this circuit is shown in

Figure 26. It is helpful in facilitating understanding of the complex nature of this circuit, particularly when dealing with Modes II and III. Table VI shows signals associated with Buffer Memory Timing Signals.

f. Voltage Requirements

Power supply P16 provides main logic plus 5 volts to this circuit board.

g. Buffer Memory Timing Circuit Component Layout

Figure 27 shows the major component layout for this circuit.

9. Drivers, Auxiliary Board 1

a. Introduction

The four auxiliary boards implemented in the DAU are, as the name implies, boards added to the DAU to correct prototype design discrepancies and add additional desirable circuits to the DAU. Auxiliary boards 1 and 2, correct design discrepancies, while auxiliary boards 3 and 4 implement desirable circuits to the DAU.

The Drivers Board (auxiliary board 1), shown in Figure 28, performs two basic functions. First it provides bus driver gates for the $\overline{\text{WE}}$, CS, and address lines sent to the Buffer Memory Boards (Section II.C.7.). Secondly, DRGØ (Ø)B1 and DRGØ(Ø)B2 are generated from DRGØ(Ø) to be used in the Buffer Memory Timing Circuit (Section II.C.8.).

b. Bus Drivers

IC-2 through IC-5 are 7438 open collector, NAND,

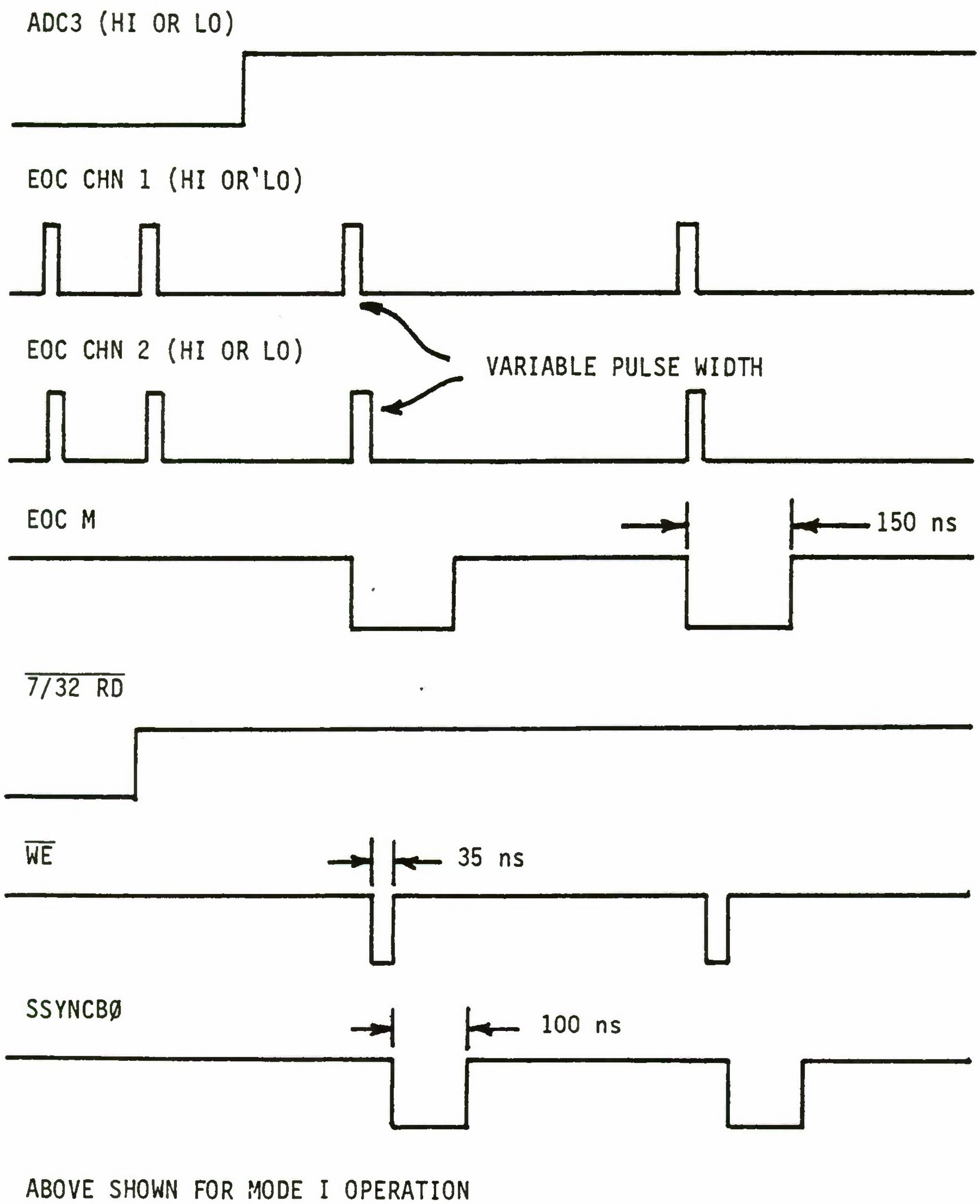



Figure 26. Buffer Memory Timing Circuit Timing Diagram (Mode I)

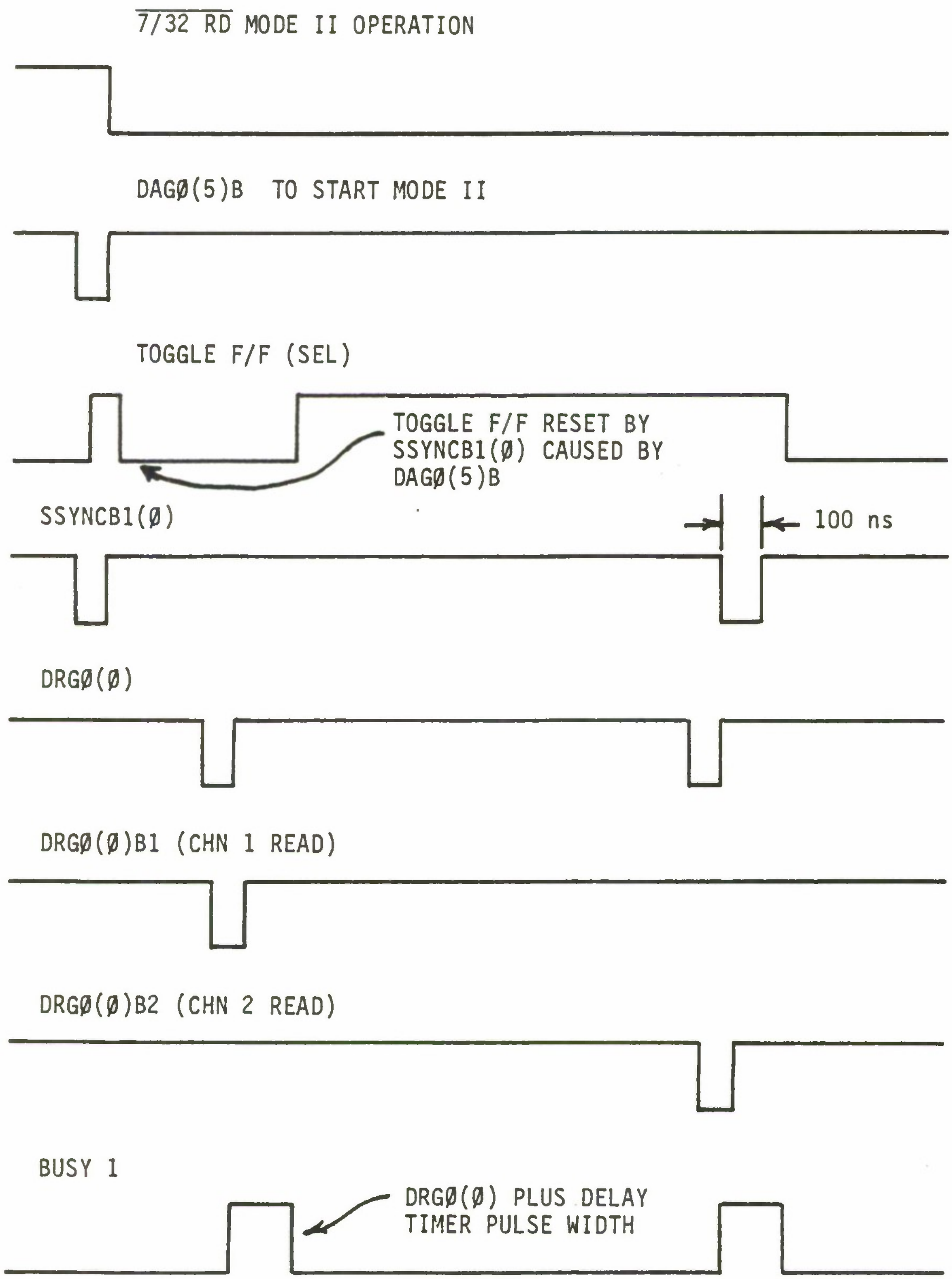



Figure 26. Buffer Memory Timing Circuit Timing Diagram (Mode II, for Mode III see Figure 20).

TABLE VI. BUFFER MEMORY TIMING SIGNALS

| Signal Name | Source | Destination | Purpose | Ref (Page) |
|---|---|---|---|---|
| EOC's | A/D Converters | Buff Mem Timing Bd | Initiate $\overline{WE}$ | Sec II.C.1/2 |
| ADC3-HI/LO | ADC Prestart Bd | Buff Mem Timing Bd | Enable EOCM | Sec II.C.4.b. |
| EOCM | Buff Mem Timing Bd | Buff Mem Timing Bd | Coincidence of EOC's | Sec II.C.8.b. |
| $\overline{WE}$ | Buff Mem Timing Bd | Buff Mem Bds | Write to RAM | Sec II.C.8.b. |
| SSYNCBØ | Buff Mem Timing Bd | Control, Output Sel | End of Cycle | Sec II.C.8.b. |
| SSYNCB1(Ø) | Inverter Bd | Buff Mem Timing Bd | Delayed SSYNCBØ | Sec II.C.10.b. |
| DRGØ | INTERDATA 7/32 ULI | Buff Mem Timing Bd | Read DAU Data | Sec II.C.8.c. |
| DRGØB1(Ø) | Driver Bd | Buff Mem Timing Bd | Output both Channels of Data | Sec II.C.8.c. |
| DRGØB2(Ø) | Driver Bd | Buff Mem Timing Bd | | Sec II.C.8.c. |
| SEL(TOGGLE F/F) | Buff Mem Timing Bd | Buff Mem Output Sel | | Sec II.C.8 |
| DAGØB1(Ø) | Buff Mem Timing Bd | Clock Chn1 Input Data | Load Diagnostic Data to DAU | Sec II.C.8.d. |
| DAGØB2(Ø) | Buff Mem Timing Bd | Clock Chn2 Input Data | | Sec II.C.8.d. |

NOTE: See Table IV for related signals.

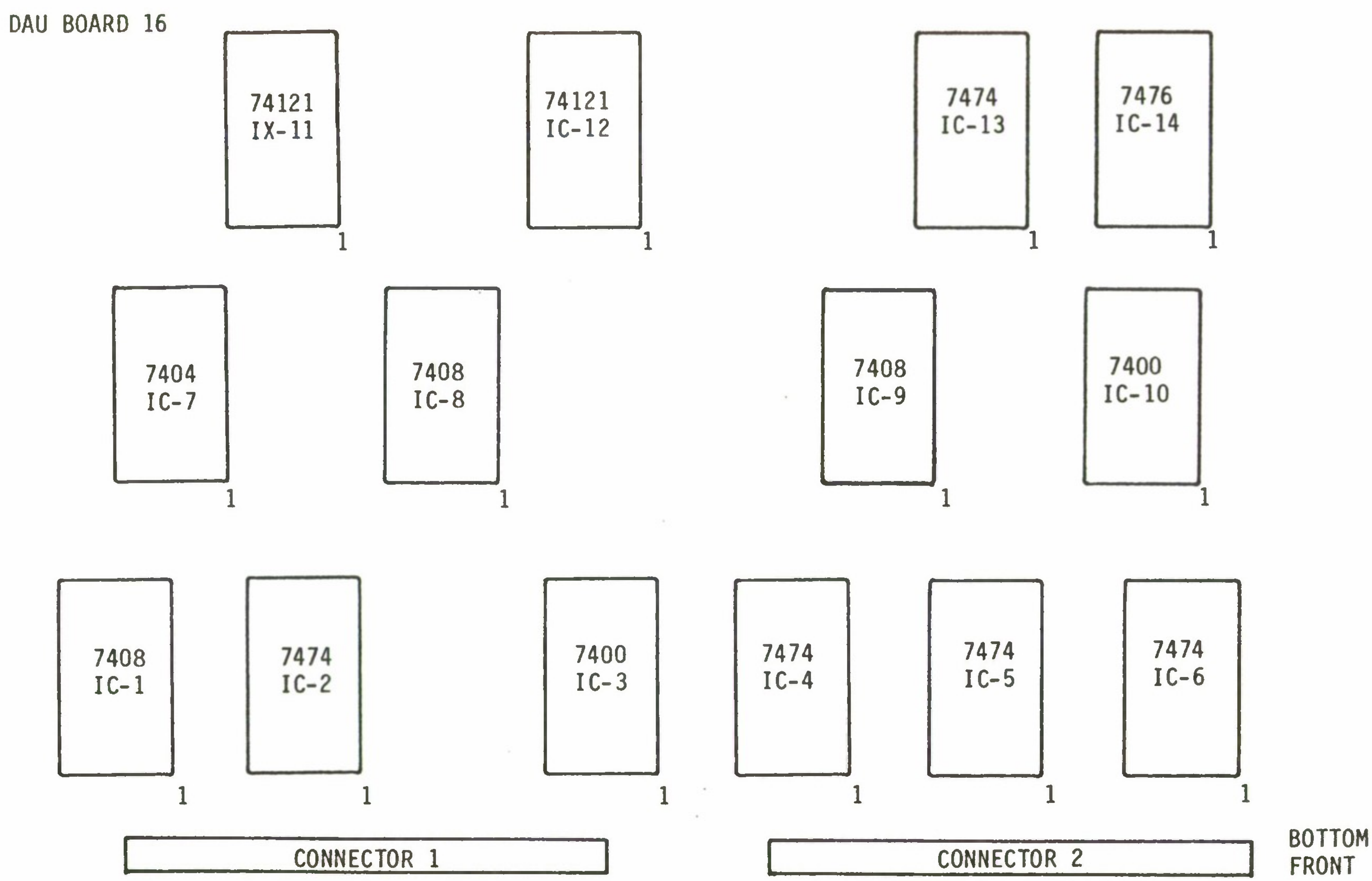



Figure 27. Buffer Memory Timing Circuit Component Layout

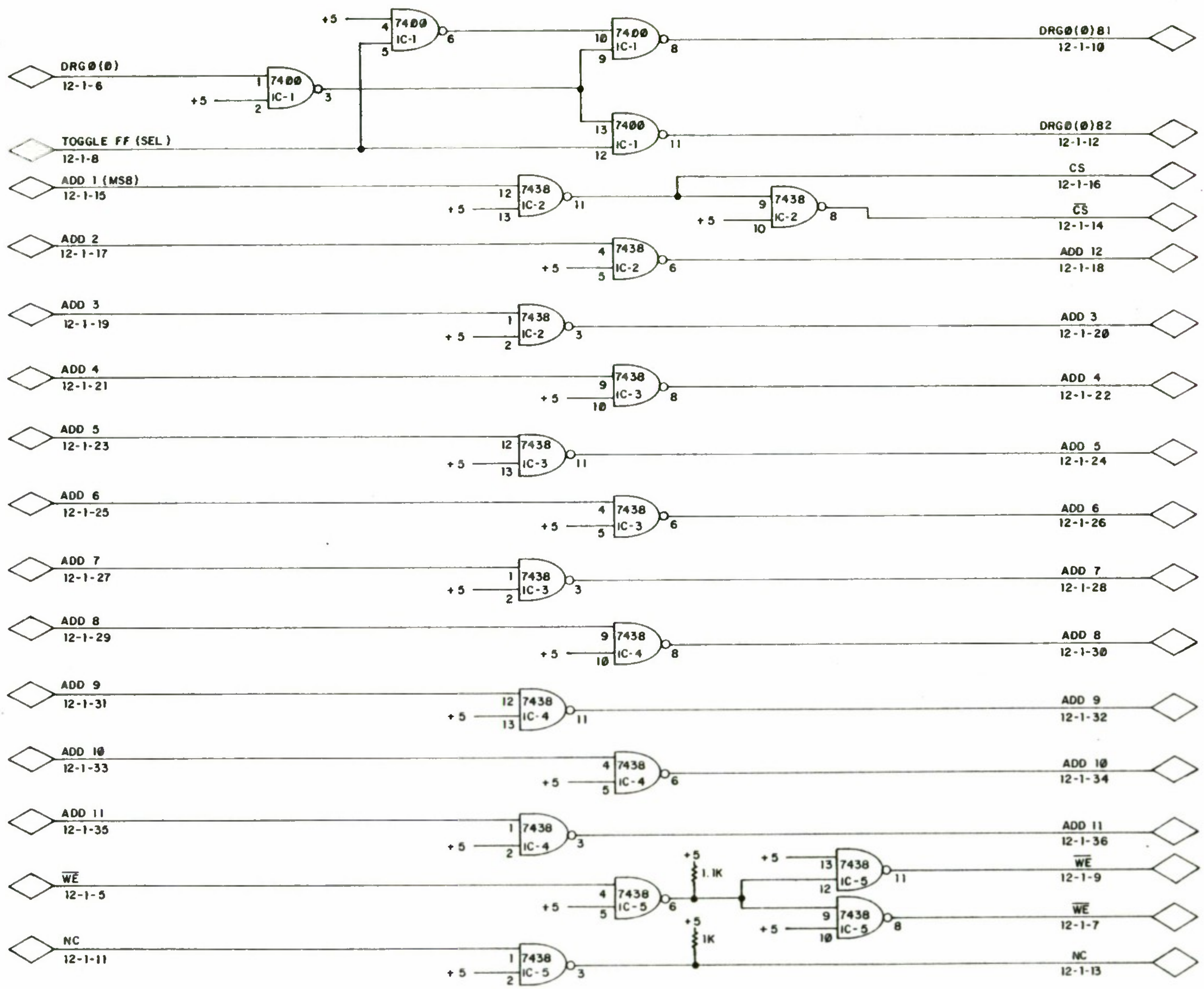



Figure 28 - Driver Circuit Auxiliary Board 1

bus, drivers, used to buffer the address inputs, the CS and $\overline{CS}$ inputs, and the $\overline{WE}$ input to the 48 93415 RAM chips on the buffer memory boards. The required pull up resistors are implemented on the buffer memory boards. Note that the inversion incurred by the NAND drivers causes no problems in the present design. Because the memory boards are always addressed by the address register on the Control Board (2 of 2), Section II.C.13., and thus driven by auxiliary board 1, no address confusion can exist. However, if the address bus to the memory boards had two sources, as in the future design (Section V.B.2.), then care must be taken to assure "WRITE" and "READ" from the same memory location.

To assure that the 35 nanosecond write enable, $\overline{WE}$, pulse is clean, it is driven by two 7438 gates on IC-5. Also, because this signal must be active low, it is first inverted through 7438 gate, pin 4 IC-5, and then split through 7438 gate, pin 12 and 7438 gate, pin 9, on IC-5. This provides one $\overline{WE}$ output for each channel of buffer memory with pull up resistors located on the memory boards.

c. Generation of DRGØ(Ø)B1 and DRGØ(Ø)B2

The generation of DRGØ(Ø)B1 and DRGØ(Ø)B2 in the four NAND gates of IC-1 is as described in Section II.C.8.2. (2).

d. Voltage Requirements

Although the auxiliary boards are implemented on VERO universal circuit boards, they have been designed to match the standard power supply pinouts used in the spare connector slots. The power for auxiliary board 1 is supplied from plus 5 volt power supply P16 located in the lower rear of equipment rack 16.

e. Driver Component Layout

The driver component layout is shown in Figure 29.

10. Inverters, Auxiliary Board 2

a. Introduction

Auxiliary board 2, Figure 3Ø, provides additional 74Ø4 inverter gates used to invert signal polarities or create delay.

b. Generation of SSYNCB1(Ø) and SSYNCB2(Ø)

74Ø4 inverter gates from IC-1, through IC-3 are used to generate delayed versions of the SSYNCBØ signal originally generated on the Buffer Memory Timing board (Section II.C.8.). By delaying SSYNCB(Ø) through the six inverters on IC-1, or approximately 6Ø nanoseconds, SSYNCB1(Ø) is generated and sent to both the Buffer Memory Output Selector Circuit (Section II.C.11.) to latch the buffer memory output data, and also returned to the Buffer Memory Timing Circuit to complete the SSYNCBØ feedback loop.

Either six or two, depending on strapping option, additional 74Ø4 inverters are added to SSYNCB1(Ø), through IC-2 and OC-3, to generate SSYNCB2(Ø). SSYNCB2(Ø) is presently wired with two additional inverters. The option for six inverters may be used in the future modified DAU. SSYNCB2(Ø)

DAU AUXILIARY BOARD 1

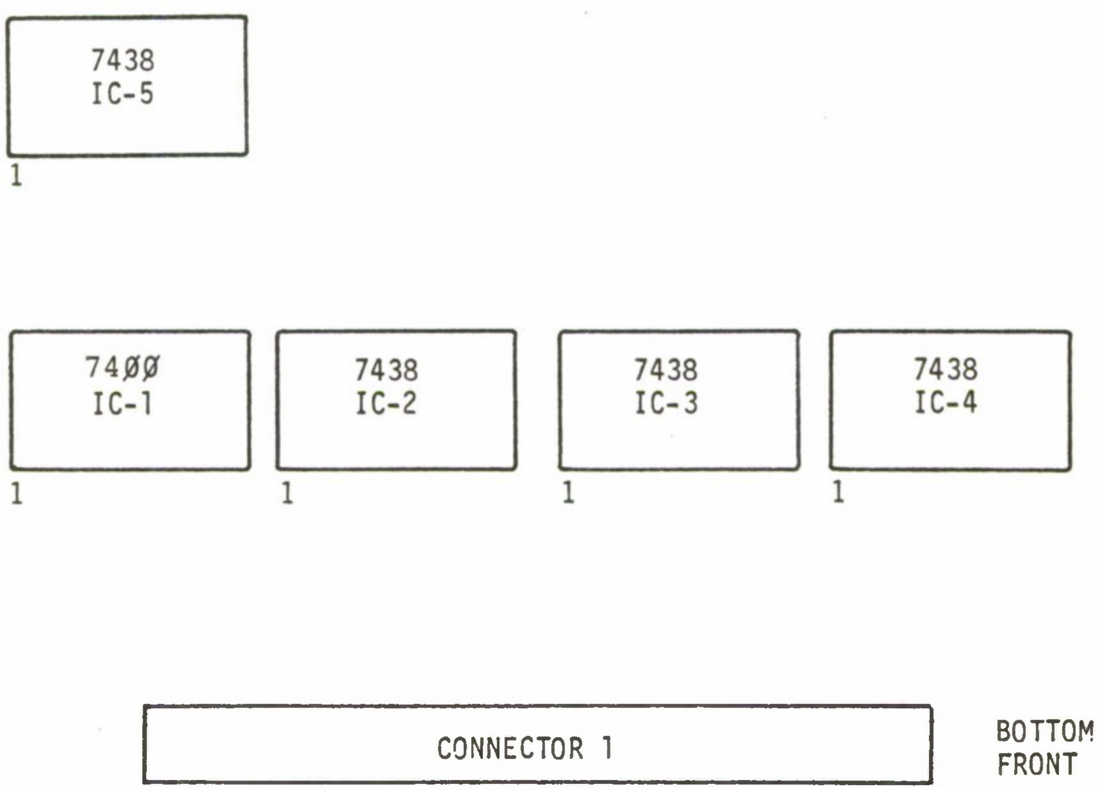



Figure 29. Driver Board Component Layout

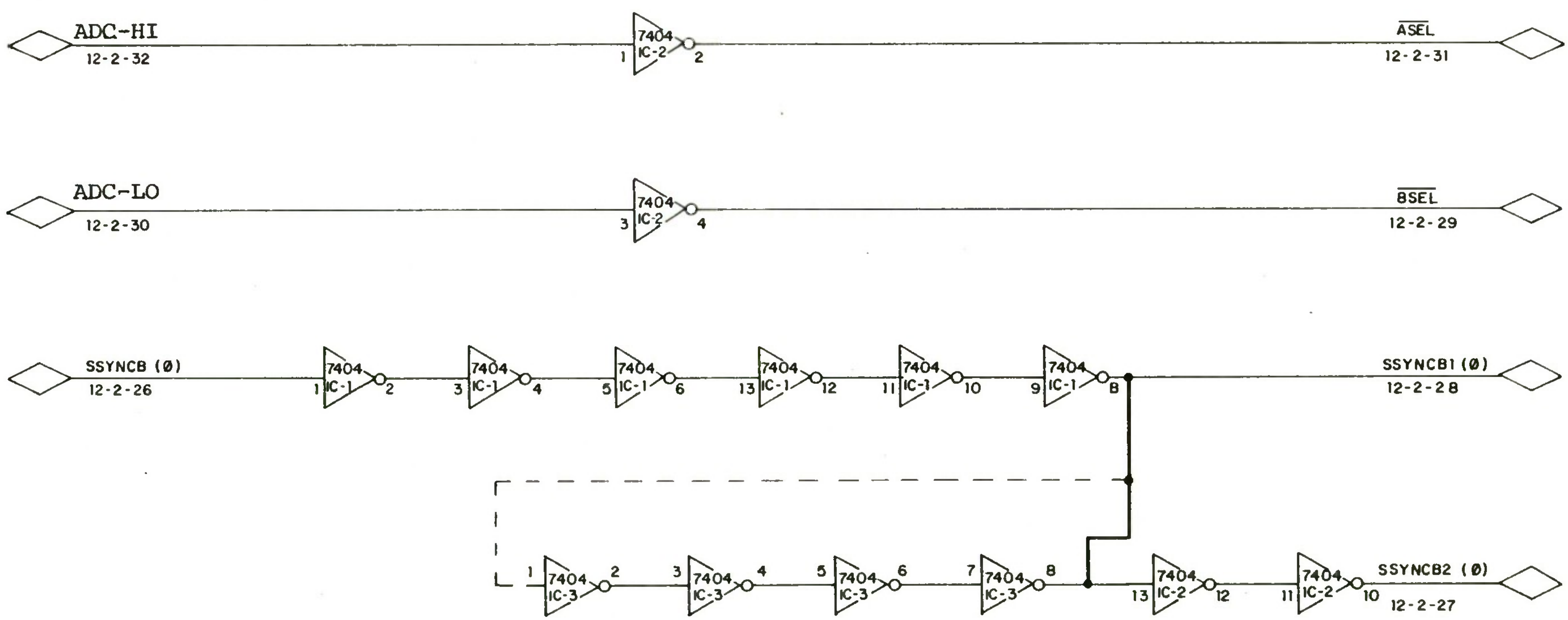



Figure 30 - Inverters Auxiliary Board 2

is used on both Control Boards ((1 of 2) and (2 of 2)) for status checking and clocking of the address and word count registers. Note that SSYNCB1(Ø) and SSYNCB2(Ø) have not been changed in polarity from the original SSYNCBØ.

c. Generation of $\overline{\text{ASEL}}$ and $\overline{\text{BSEL}}$

By inverting the ADC-HI and ADC-LO inputs of edge connector pins 12-2-32 and 12-2-3Ø respectively, ASEL and BSEL are generated and used in teh Buffer Memory Input Selector Circuit as discussed in Section II.C.6.b.

d. Voltage Requirements

The auxiliary board 2 is supplied plus 5 volts from the main logic power supply, P16, located in the lower rear of equipment rack 16.

e. Inverter Component Layout

The auxiliary board 2 component layout is shown in Figure 31.

11. Buffer Memory Output Selector Circuit

a. Introduction

The Buffer Memory Output Selector Circuit, DAU board 14 is shown in Figure 32. This circuit provides a means of outputting both channel 1 and channel 2 data to a single 16 bit output port, for either the INTERDATA 7/32 or the AP-12ØB Array Processor. Onboard bus drivers are provided for both receiving devices.

DAU AUXILIARY BOARD 2

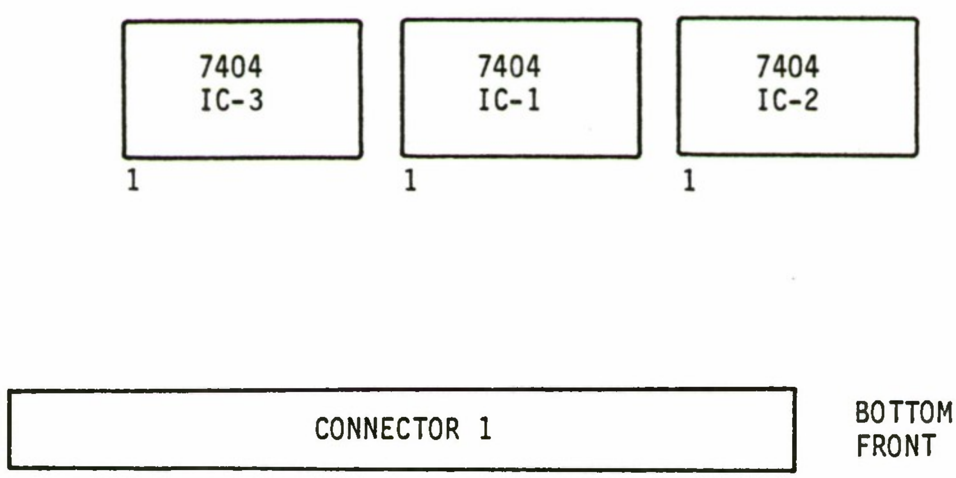



Figure 31. Inverter Board Component Layout

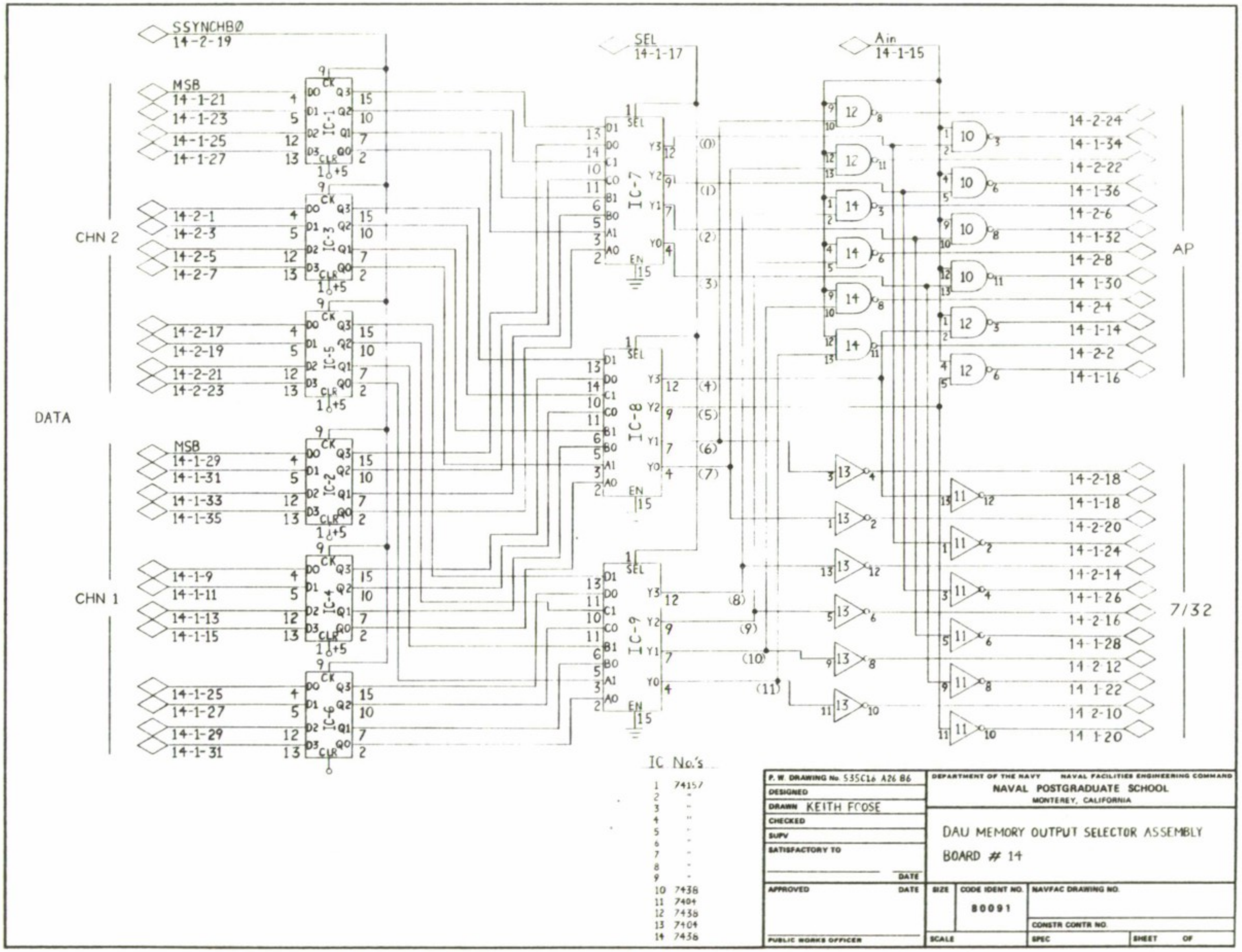


Figure 32 - Buffer Memory Output Selector Circuit

b. Latched Output Data

Output data for buffer memory data from channel 1 and channel 2 is parallel latched on the output selector board into six 74175 four bit latches, IC-1 through IC-6, on the trailing edge of SSYNCB1(Ø) pulse (from auxiliary board 2, Section II.C.12.). This data then remains latched through the entire cycle between SYNCB1(Ø) pulses, which allows adequate time to "read" the data out to the receiving device.

c. Output Multiplexer

Three 74157 quad 1 of 2 multiplexers, IC-7 thru IC-9 are used to select data (one channel at a time) to the output port. The SEL input, pin 14-1-17, generated on the Buffer Memory Timing board (Section II.C.8.) correctly toggles both channels of data out to the port during the "read" (mode II) cycle.

d. Output Bus Drivers

Parallel 12 bit bus drivers for the INTERDATA 7/32 data in bus (DIN lines), and the AP-12ØB bi-directional data bus are included on this board. Both sets of bus drivers are tied in parallel to the output multiplexer chips. Although the DAU can presently output only to the INTERDATA 7/32 DIN lines, IC-1Ø, IC-12 and IC-14, 7438 open collector NAND bus driver gates will provide drive for data onto the AP-12ØB's IOP-16 I/O data bus (future application). The bus drivers for the AP-12ØB are compatible with Digital Equipment Corporation Unibus data bus requirements as used by FLOATING POINT

SYSTEMS in the IOP-16. In both cases data is left justified to put 8 or 12 data bits into a field of 16 bits with bit "Ø" as most significant bit (MSB).

e. Output Selector Timing

Figure 33 shows the timing relationships for this circuit.

f. Voltage Requirements

The power to this circuit is supplied by plus 5 volt main logic power supply P16, located in the lower rear of equipment rack 16.

g. Output Selector Component Layout

The major component layout for this circuit is shown in Figure 34.

12. Control Board (1 of 2), DAU Interface

a. Introduction

Control Board (1 of 2) and Control Board (2 of 2) are two parts of one major DAU circuit designed to interface the DAU to its controlling processor, which is presently the INTERDATA 7/32. Together, Control Boards (1 of 2) and (2 of 2) receive, via the ULI board, output data (DOT lines), control out signals (COT lines) and active low interfacing pulses, data available, gated (DAGØ), and data request, gated (DRGØ). Through this interface with the INTERDATA 7/32, the DAU is precisely controlled to operate as documented, and send back DAU status to the status input lines (SIN lines) of the INTERDATA. The Control board (1 of 2) performs two

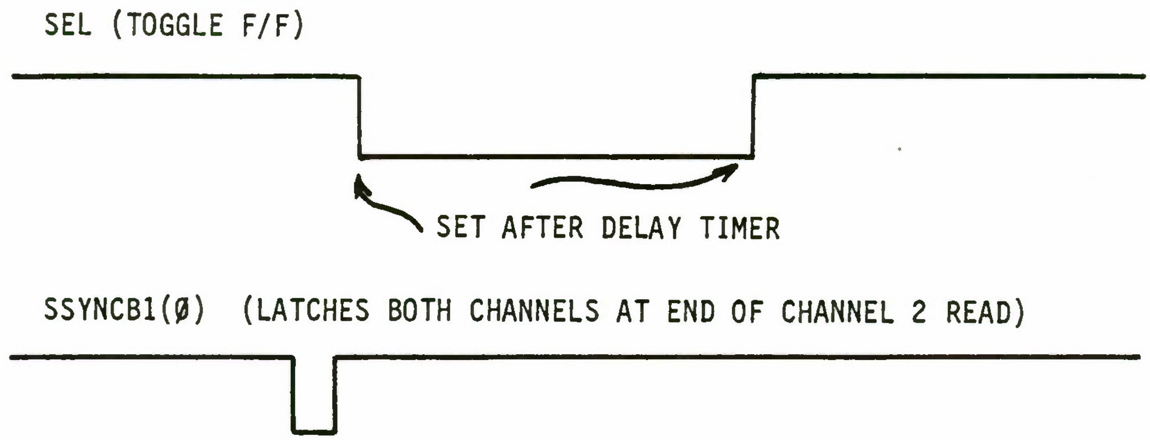



Figure 33. Buffer Memory Output Selector Timing Diagram

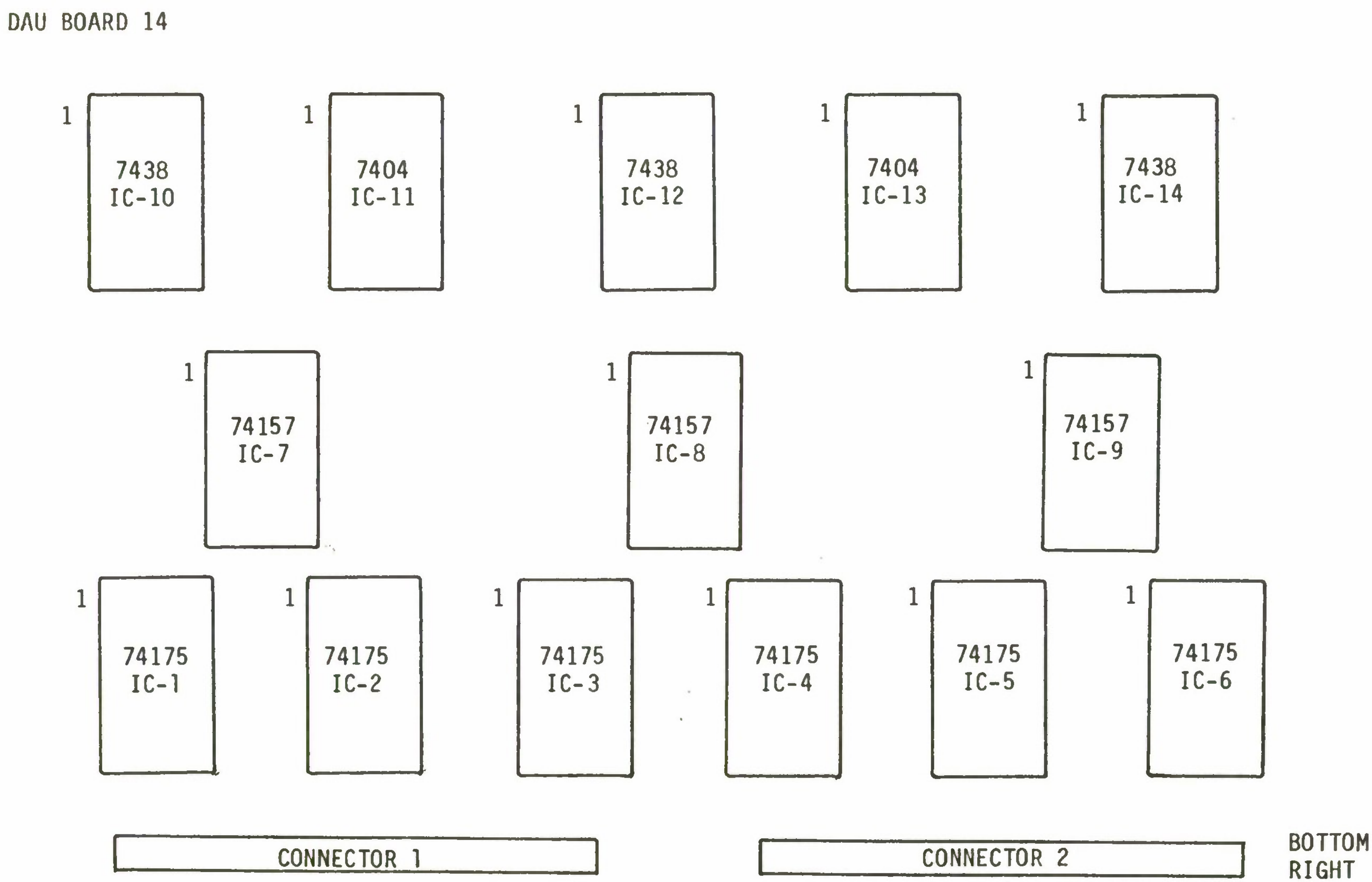



Figure 34. Buffer Memory Output Selector Component Layout

basic functions. First it receives the COT line signals and the DAGØ pulses, and second it provides for the SIN lines, the DAU status. See Figure 35.

b. DAGØ Routing

COT lines Ø4Ø through Ø7Ø are recieved with inverter receivers, 74Ø4 gates on IC-1, and sent to the four address input, pins 2Ø through 23, of the 74154 1 of 16 multiplexer, IC-2. Using the DAGØ pulse on pin 18, data in, of IC-2, the software controlled states of COT Ø4Ø through COT Ø7Ø provides DAGØ(Ø) through DAGØ(5). This technique allows the DAGØ pulse to be distributed throughout the DAU to trigger various events under INTERDATA 7/32 control.

c. Status Register

The status register supplies four bits (SIN Ø4Ø, SIN Ø5Ø, SIN Ø6Ø and SIN Ø7Ø) of status information to the INTERDATA 7/32. These bits are individually generated on Control Board (1 of 2) and only have meaning as used by the software programs that operate the DAU. The term status register indicates more than one status bit.

(1) BUSY Ø, SIN Ø4Ø. The BUSY Ø status bit, fed-back to the INTERDATA on the SIN Ø4Ø line, is used to inform the INTERDATA that the DAU is in either of two conditions, defined as a busy state.

The first condition is during the acquisition mode (mode I) when either the high or low speed A/D converters are on. In this condition either the ADC-HI or ADC-LO inputs,

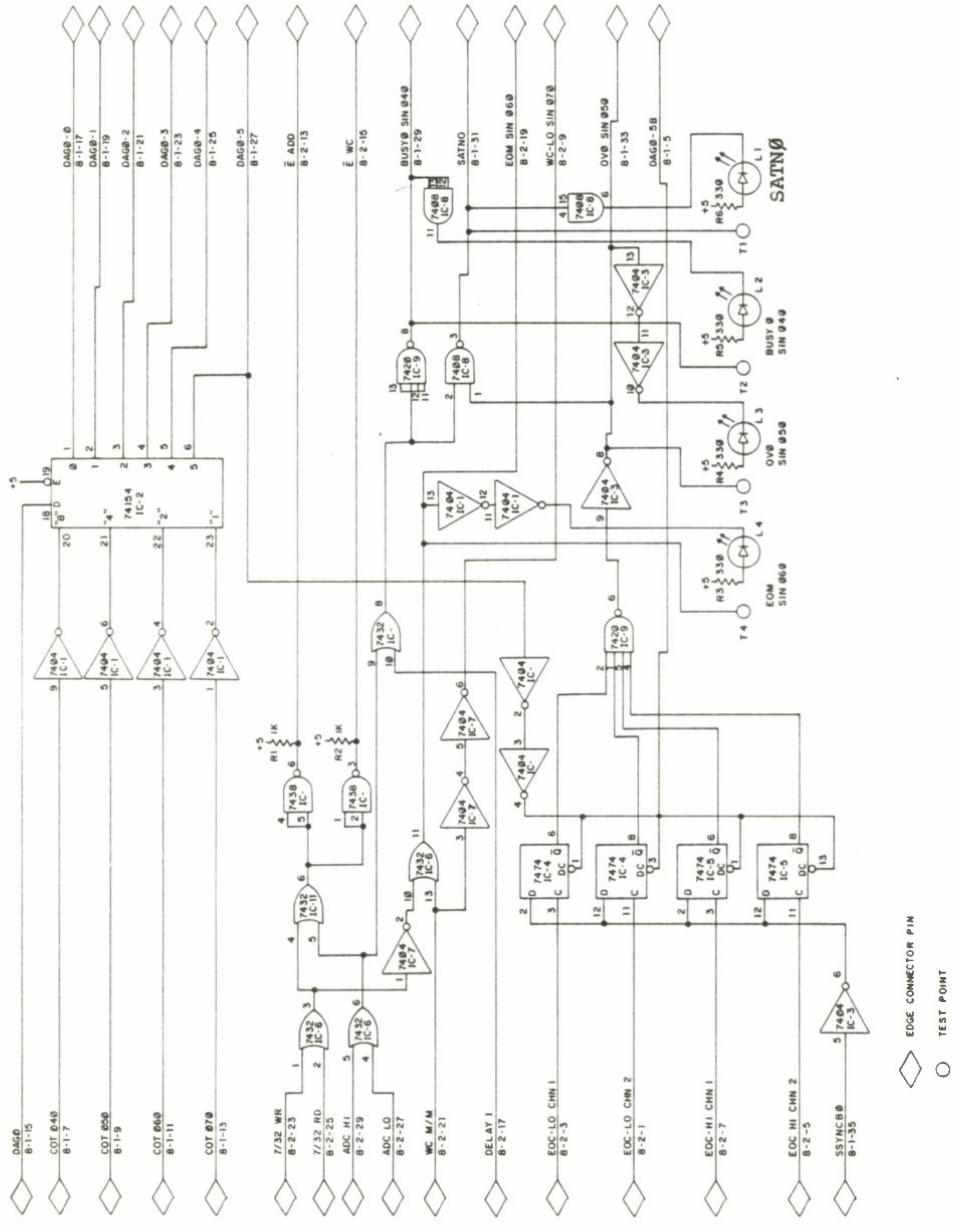



Figure 35 - Control Board (1 of 2) Circuit

edge connector pins 8-2-29 or 8-2-27 respectively, will be asserted high. That high will be OR'ed through 7432 gate, pins 4 or 5, IC-6, and OR'ed a second time through 7432 gate, pin 9, IC-11, and finally inverted to active low through 742Ø gate, pin 8 of IC-9, where it is fed off the board on edge connector pin 8-1-29. The BUSY Ø status also light LED on board indicator, L2, through 74Ø8 gate, pin 11, IC-8, used as a buffer. Test point T2 allows access to the BUSY Ø status line.

The second BUSY Ø condition is set by the OR of the DELAY 1 input, pin 8-2-17, through 7432 gate, pin 1Ø, IC-11, and on through as described for the first condition. DELAY 1 is asserted by BUSY 1 from the Buffer Memory Timing Circuit as described in Section II.C.8.c. This condition exists during the transfer of data to or from the INTERDATA (mode II or mode III) during the buffer memory access time and the additional built in delay.

(2) OVØ, SIN Ø5Ø. This status bit is implemented to detect an end-of-convert (EOC), from either of the operational ADC channels, prior to the completion of memory access for the previous EOC cycle. This situation could occur either as a result of operating the DAU at too fast a sample rate for the chosen ADC, or due to a timing fault as a result of component failure.

OVØ (OVER RUN) is generated by four 7474 D flip-flops, IC-4 and IC-5 used as timing comparators during the acquisition mode (mode I) only. To initialize the D flip-flops and assure the correct starting posture, DAGØ(5), pin 6, IC-2, via two 74Ø4 inverter gates on IC-3, direct clears all four flip-flops which asserts their $\overline{Q}$ outputs high. All four $\overline{Q}$ outputs NAND together in 742Ø gate IC-9, which goes low on pin 6, only when all four inputs are high. The NAND output is inverted by 74Ø4 gate, pin 9, IC-3, to supply test point T3 and the OVØ SIN Ø5Ø output, pin 8-2-19. Two additional inverters on IC-3, buffer OVØ to indicator LED, L3. SSYNCB2(Ø), generated on auxiliary board 2, is input to the Control Board (1 of 2), pin 8-1-35, routed via 74Ø4 inverter gate, pin 5, IC-3, and applied as an active high signal to the D input of all four D flip-flops. Additionally each flip-flop is clocked by one of the A/D converter active low EOC signals. If any one of the four flip-flops receive the trailing edge of an EOC signal while the SSYNCB2(Ø) input is asserted high, a low will be latched to the $\overline{Q}$ output and hence cause the NAND output to go high, asserting that an OVER RUN has occured.

(3) EOM, SIN Ø6Ø. End-of-medium (EOM) is asserted when the work count (WC) register goes to zero (Section II.C.13.g.) with a transfer request pending. This condition would indicate that the DAU had transferred out of or into storage (mode II or mode III) all of the data words defined by a particular block transfer. If the INTERDATA continued to try and transfer data from or to DAU buffer memory

it would either be taking bad data (mode II or possibly overwriting memory locations during the diagnostic mode (mode III).

EOM is generated by combinational logic using the 7/32 WR, pin 8-2-23, the 7/32 RD, pin 8-2-25, and the WC M/M, pin 8-2-21, inputs. 7/32 WR and 7/32 RD are OR'ed in 7432 gate, pins 1 and 2, IC-6, then inverted through 74Ø4 gate, pin 1, IC-7, and applied to pin 12 of 7432 OR gate, IC-6. WC M/M is applied to that same 7432 gate pin 13, with the output pin 11 providing the EOM status bit pin 8-2-19. During transfer activity (mode II and mode III) pin 12 of IC-6 will be low. If the WC register reaches zero, WC M/M will go low to apply active low EOM. EOM is also applied to indicator LED, L4, via buffer inverters on IC-1. Test point, T4, provides EOM access.

(4) WC-LO, SIN Ø7Ø. Word count low (WC-LO) is the WC M/M input buffered by inverters on IC-7 to provide full time status of the word count register regardless of mode of operation. This status bit has not been physically wire wrapped to the SIN Ø7Ø line; however, the edge connector pin 8-2-29 has been provided for future application.

d. Generation of SATNO

The SATNO output (send attention), active low signal, is an interrupt bit sent to the INTERDATA 7/32, ULI Board to request that the INTERDATA respond to the DAU pending word transfer to or from the DAU. An interrupt status is sent to the INTERDATA whenever SATNO is low.

SATNO is generated as the active low OR of BUSY Ø and OVØ through 74Ø8 gate, pin 1 and 2 of IC-8. Normally SATNO is sent whenever BUSY Ø is not sent. In addition SATNO is sent on an OVØ condition to cause an immediate interrupt to the INTERDATA rather than wait for polling of the status register. LED, L1, provides on board indication and test point, T1, provides easy access to SATNO.

e. Generation of $\overline{E}$ ADD and $\overline{E}$ WC

The address and word count registers on Control Board (2 of 2) are enabled by $\overline{E}$ ADD and $\overline{E}$ WC generated on Control Board (1 of 2) pins 8-2-13 and 8-2-15 respectively. Using the OR'ed combination, IC-6 and IC-11, of the 7/32 RD, ADC-HI and ADC-LO, $\overline{E}$ ADD and $\overline{E}$ WC are asserted active low during all modes of the DAU. The purpose of these two signals is to prevent the WC and ADD registers from incrementing during DAU set up.

f. Voltage Requirements

This circuit is supplied power from the plus 5 volt main logic power supply, P16, located in the lower rear of equipment rack 16.

g. Control Board (1 of 2) Component Layout

Figure 36 shows the component layout for this circuit.

13. <u>Control Board (2 of 2), DAU Interface</u>

a. Introduction

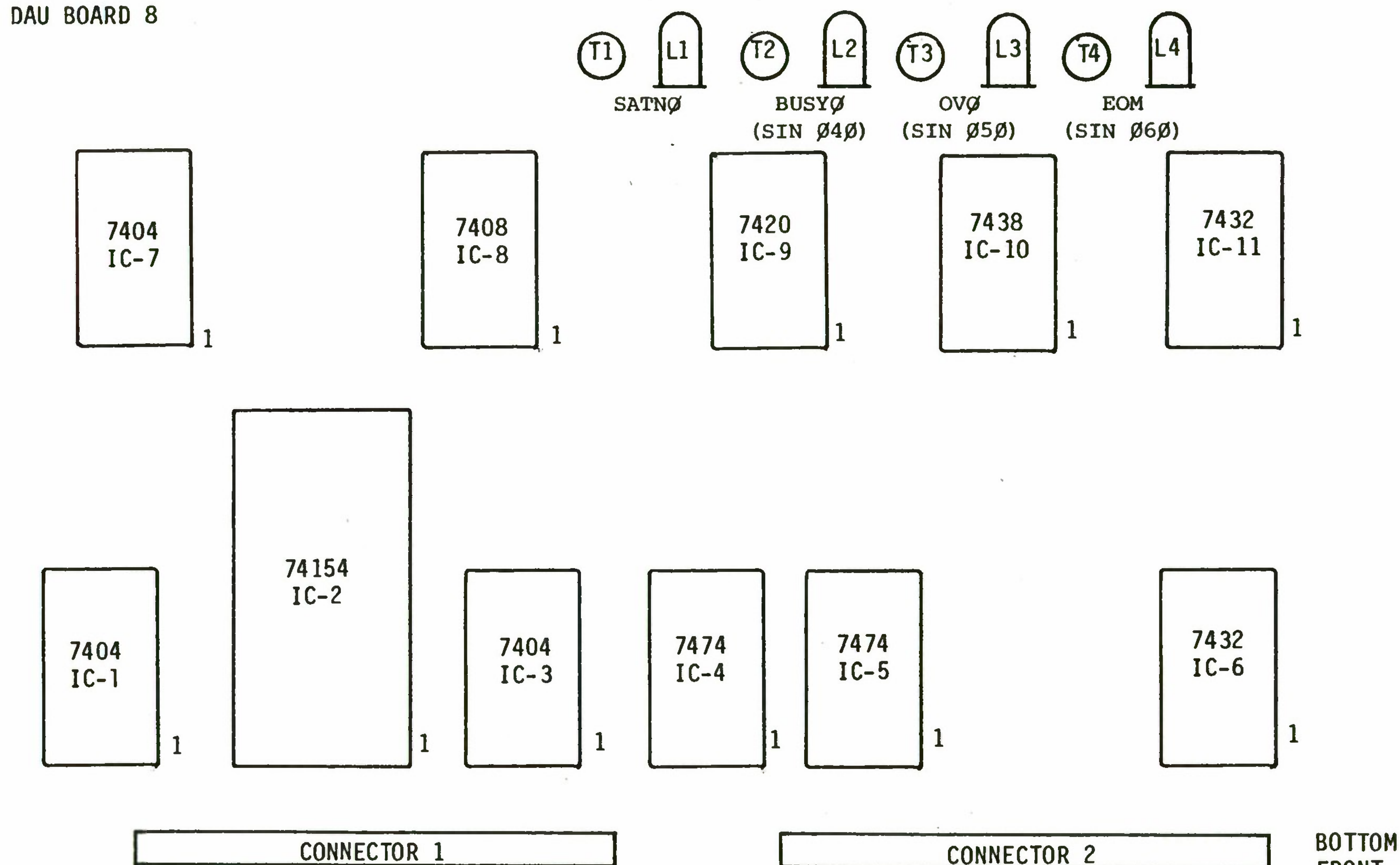



Figure 36. Control Board (1 of 2) Component Layout

Control Board (2 of 2), Figure 37, implements the second of two boards that interface the DAU with the INTERDATA 7/32. This board, DAU board 1Ø, contains the INTERDATA data out line (DOT lines) inverter receivers, and five registers, controlled by the INTERDATA 7/32, that specify DAU activity.

b. Data Input

Control Board (2 of 2) provides sixteen 74Ø4 inverter gates, IC-1 through IC-3, to receive data input from the INTERDATA 7/32, via the ULI board. The inverter receivers in addition to buffering the data lines, convert the input to positive logic.

c. DAGØ Pulse

The data in lines (DOT) are parallel wired to all five registers on Control Board (2 of 2). To organize which register is loaded by the available data, each register is individually given a load command by DAGØ(1) through DAGØ(5), generated by Control Board (1 of 2), Section II.C.12. These DAGØ(X) active low commands are routed versions of the data available, gated (DAGØ) command asserted by the ULI for each data transfer to the DAU.

d. Range Register

The RANGE register consists of one 74175 quad latch, IC-4. When clocked by DAGØ(1), it latches available data from DOT 121 through DOT 151. This latched data provides a BCD value that determines the range of frequencies the SM-1Ø1 frequency synthesizer can operate in. To operate

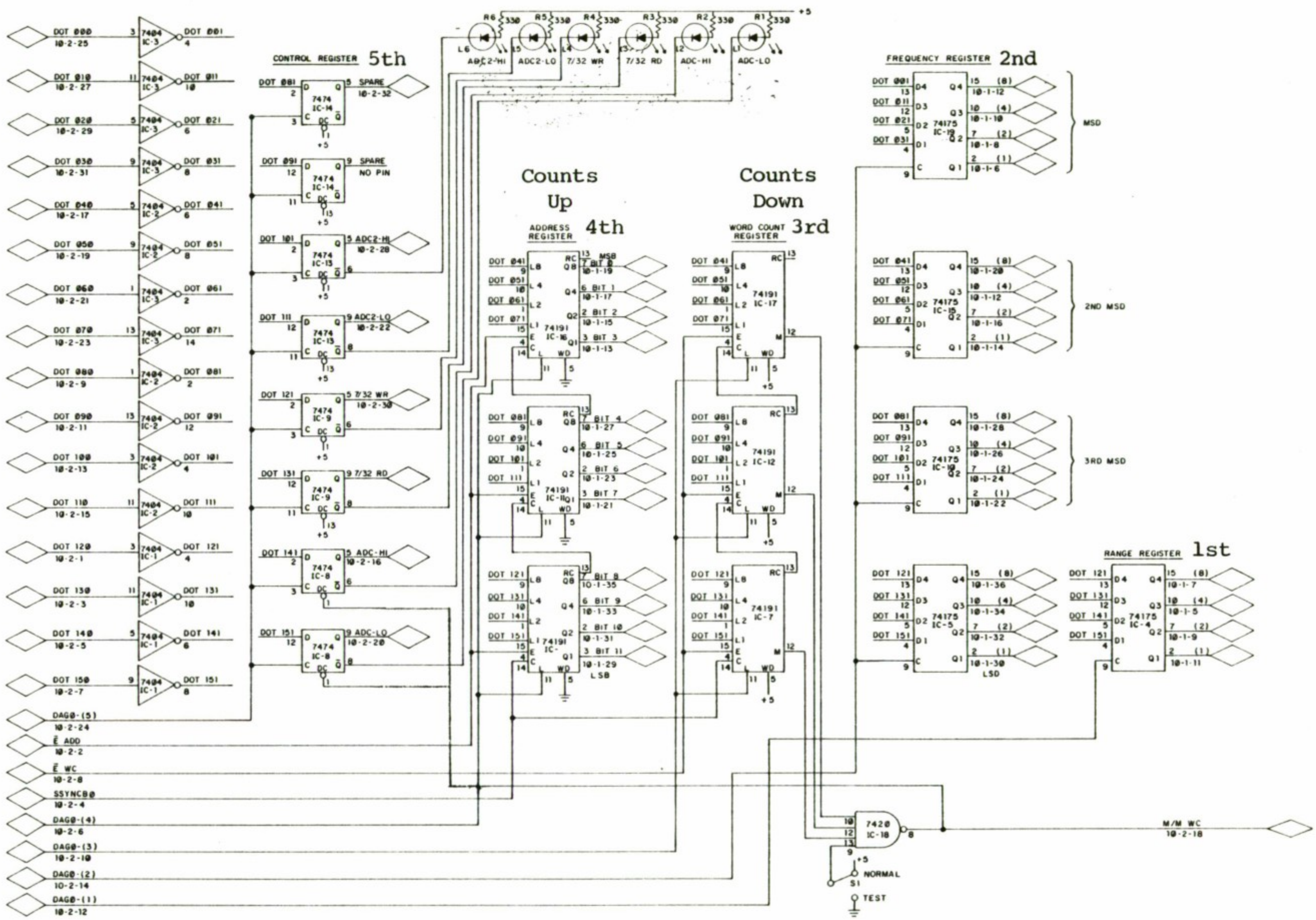



Figure 37 - Control Board (2 of 2) Circuit

the DAU at a sample rate other than that allowed by a given range setting, the RANGE register must be reloaded by INTERDATA 7/32 program control.

e. Frequency Register

Four 74175 quad latches, IC-5, IC-1Ø, IC-15 and IC-19, make up the FREQUENCY register. When clocked by DAGØ(2) the FREQUENCY register latches data from all 16 DOT lines to provide four BCD digits of data to the SM-1Ø1 for frequency setting. The frequency and range settings for the SM-1Ø1 are contained in Appendix 3. The sample rate of the DAU will be as specified by the FREQUENCY register until specifically changed by program control from the INTERDATA 7/32.

f. Word Count Register

The WORD COUNT register (WC), allows the DAU to maintain a pre-set word count capability, used during the acquisition mode (mode I) to stop A/D conversion at the completion of the pre-set block size. Three 74191 up/down 4 bit counters, IC-7, IC-12 and IC-17, make up the WC register. DAGØ(3) loads the data available on DOT Ø41 through DOT 151, which determines the maximum value of the acquisition block. When $\bar{E}$ WC is low the WC register counts down one value for each SSYNCB2(Ø) received (Section II.C.8.). SSYNCB2(Ø) clocking is only applied to pin 14 of IC-7 (LSB) and then progressed up the register by the ripple count (RC) output pin on each chip. When the WC register has been counted down to zero (all bits zero) each chip's M/M output, pin 12, goes high.

All three M/M high levels plus a test switch, IC-18, outputs M/M WC, pin 1Ø-2-18, to Control Board (1 of 2). M/M WC is also applied back to the CONTROL register to direct clear the ADC-HI and ADC-LO flip-flops thus terminating acquisition for a particular block of data. Note, during special conditions, such as trouble-shooting, the DAU can be caused to run indefinitely in an acquisition mode by switching S1 to the TEST position and thereby denying that M/M WC ever be asserted low. The WC register must be reset by program control for each block of acquisition (mode I, II and III).

g. Address Register

The ADDRESS register (ADD), implemented just as was the WC register, is pre-set by data lines DOT Ø41 through DOT 151 when loaded by DAGØ(4). The ADD register is set to count up and thus provides to the buffer memories incremented addresses starting from the pre-set address. Just as the WC register, the ADD register clocks up one value for each SSYNCB2(Ø) received when $\overline{\text{E}}$ ADD is low. The ADD register must be reset by program control for each block of acquisition (mode I, II, and III). Note, 12 bits of ADD and WC allows a complete count of 4Ø95; however, bit zero (MSB) is not used, limiting the largest count in the ADD and WC registers to 2Ø47 which is compatible with the size of buffer memory.

h. Control Register

Eight D flip-flops, IC-8, IC-9, IC-13, and IC-14, are used as individually resettable latches for mode control of the DAU. IC-14 is presently not used, but rather is available as two spare latches. IC-8, loaded from data lines, DOT 141 and DOT 151, provides the ADC-HI and ADC-LO outputs. These two signals are direct cleared by M/M WC low. IC-9, loaded from data lines DOT 121 and DOT 131, provides the 7/32 WR and 7/32 RD outputs, IC-13, loaded from data lines DOT 1Ø1 and DOT 111, provides the ADC2-HI and ADC2-LO outputs. Each of these signals are individually discussed in other sections of the DAU OPERATION. The CONTROL register is loaded by DAGØ(5), which is the last step in the set-up seuenqe that starts the DAU in any of its modes of operation. Except for ADC-HI and ADC-LO all output values remain asserted until reloaded by program control from the INTER-DATA 7/32.

i. Voltage Requirements

This circuit is powered by plus 5 volts from the main logic power supply located in the lower rear of equipment rack 16.

j. Control Board (2 of 2) Component Layout

Figure 38 shows the component layout for this board. Table VII lists the Control Board Signals.

14. <u>Power Supplies</u>

a. Introduction

The DAU power requirements have been satisfied using eight individual power supplies. This liberal use of power supplies assures maximum isolation between the two

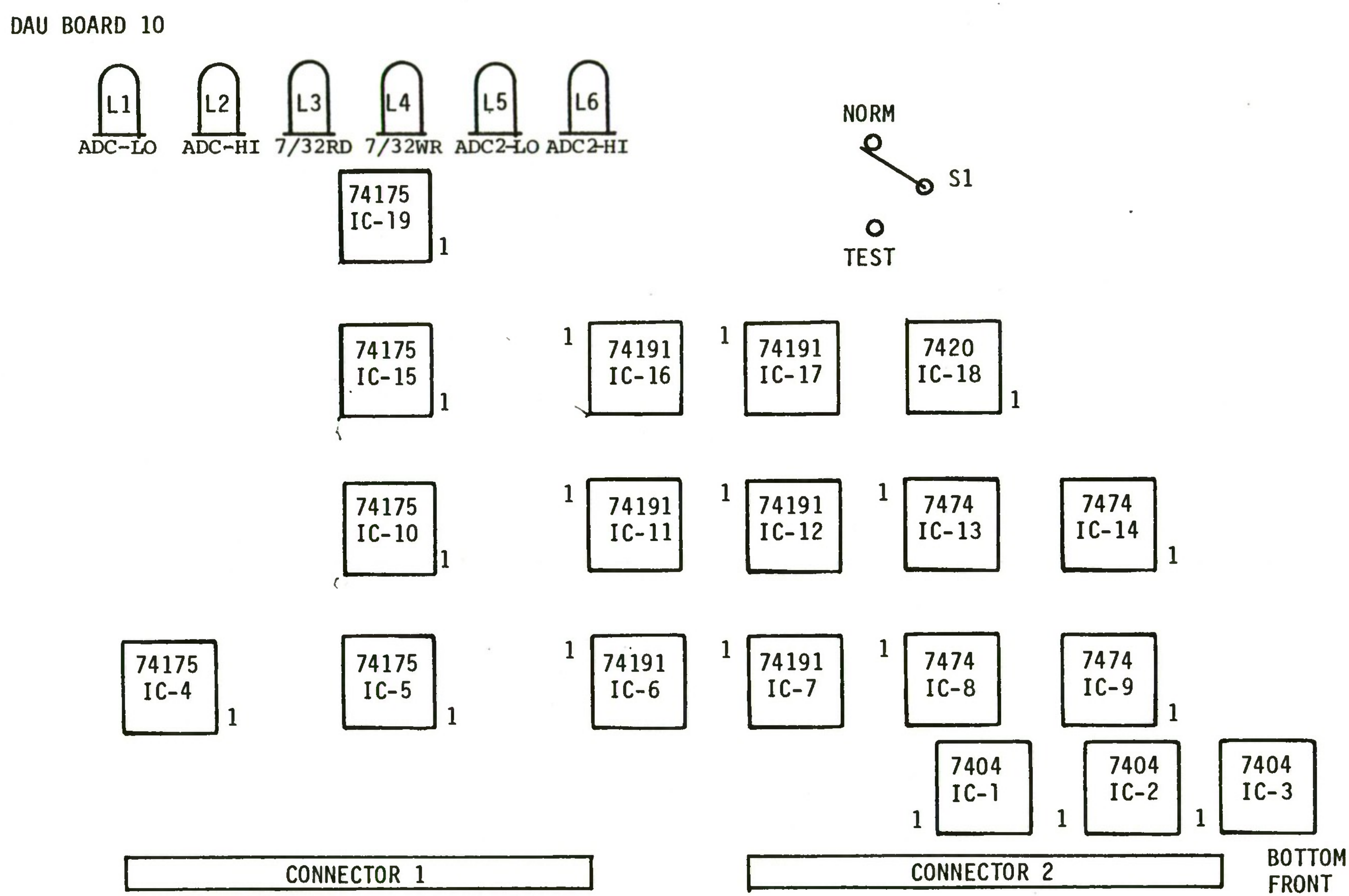



Figure 38. Control Board (2 of 2) Component Layout

TAB[illegible] BOARD SIGNALS

| Signal Name | Source | Destination | Purpose | Ref |
|---|---|---|---|---|
| 7/32 RD | Control Board (2 of 2) | Buff Mem Timing Bd | Control Mode II | Sec II.C.13.h |
| 7/32 WR | Control Board (2 of 2) | Control Board (1 of 2) | Control Mode III | Sec II.C.13.h. |
| ADC's | Control Board (2 of 2) | ADC Prestart Bd | Control Mode I | Sec II.C.13.h. |
| ADC2's | Control Board (2 of 2) | ADC Prestart Bd, ADC Timing Bd | Control Prestart | Sec II.C.13.h. |
| WC M/M | Control Board (2 of 2) | Control Board (1 of 2) | End of Acquisition Block | Sec II.C.13.f. |
| $\overline{E}$ ADD | Control Board (1 of 2) | Control Board (2 of 2) | Enable Address Reg | Sec II.C.12.e. |
| $\overline{E}$ WC | Control Board (1 of 2) | Control Board (2 of 2) | Enable Word Count Reg | Sec II.C.12.[illegible] |
| DAGØ (1 Thru 5) | Control Board (1 of 2) | Control Board (2 of 2) | Load Register (1-5) | Sec II.C.12.[illegible] |
| DAGØ(Ø) | Control Board (1 of 2) | Buff Mem Timing Bd | Load Diagnostic Data | Sec II.C.12.b. |
| BUSYØ (SN Ø4Ø) | Control Board (1 of 2) | 7/32 ULI Bd | DAU Busy Status | Sec II.C.12.c. |
| OVØ (SIN Ø5Ø) | Control Board (1 of 2) | 7/32 ULI Bd | DAU Overrun Status | Sec II.C.12.c. |
| EOM (SIN Ø6Ø) | Control Board (1 of 2) | 7/32 ULI Bd | DAU End of Medium Status | Sec II.C.12.c. |
| SATNO | Control Board (1 of 2) | 7/32 ULI Bd | DAU to 7/32 Interrupt | Sec II.C 12.d |
| SSYNCB2(Ø) | Inverter Bd | Control Board (2 of 2) | Clock ADD and WC Reg | Sec II.C.10.b. |

data acquisition channels.

b. DAU Backplane Power Supplies

Three of the eight power supplies, P17, P2Ø, and P21, are physically mounted on the DAU backplane. These power supplies, located as shown in Figure 39, provide plus and minus five volts to the channel one and channel two ADC and SHM modules. P21 is plus 5 volts channel 2, P2Ø is plus 5 volts channel 1, and P17 is minus 5 volts for channel 1 and channel 2. Due to the small power consumption, the common minus 5 volt power supply is not considered an isolation problem.

c. Rack 16 Power Supplies

Power supplies P16, P18, and P19 are located in the lower rear of equipment rack 16. Each power supply feeds a terminal strip, mounted near the power supplies, easily accessible for connection to the DAU. P16 is plus 5 volt main logic power, P18 is plus and minus 15 volt power to channel 1 ADC boards, and P19 is plus and minus 15 volt power to the channel 2 ADC boards.

d. Rack 17 Power Supplies

Power supplies P4 and P5 are located in the lower rear of equipment rack 17. These supplies feed a terminal strip arrangement as in rack 16. P4 is plus 24 volts supplied to the SM-1Ø1, DAU frequency synthesizer, and P5 is plus 1Ø volts supplied to the SM-1Ø1.

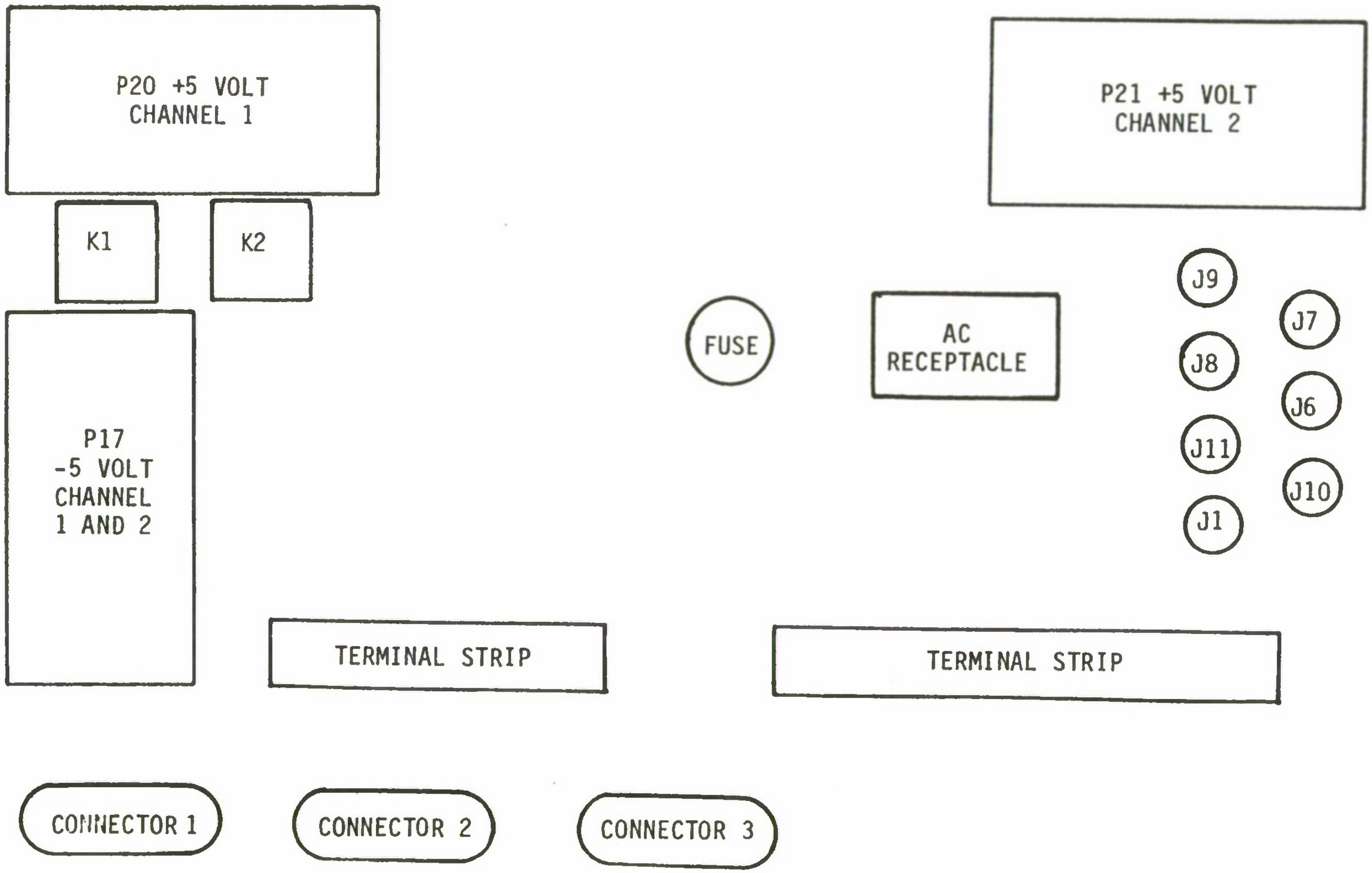



Figure 39. DAU Backplane Component Layout

e. Protect Relays

Relays k1 and k2 shown in Figure 39, switch on and off all DAU power supplies, except P4 and P5, with the AC supply to the DAU. This configuration is designed to remove power from the DAU boards in the event of DAU AC loss. Rack 16 blower fans are connected to the same AC supply, thus insuring that DAU power is removed when cooling air is lost.

A quick determination of DAU power supply status is available from the top of the DAU by inspecting the eight LED power supply indicators on the ADC protect board (Section II.C.5.).

## D. DAU TEST PANEL

### 1. Introduction

As with any device designed for computer control, normal operation of the device happens at rates not easily observable. To allow control of the DAU to occur at human speed, under human control, the DAU Test Panel was designed and implemented to directly replace the INTERDATA 7/32 DAU interface. The Test Panel, when connected to the DAU in place of the INTERDATA, then in effect becomes the controlling computer for the DAU.

### 2. DAU Test Panel Operation

The DAU Test Panel circuit, shown in Figure 40, consists of a set of single pole, single throw switches, one each,

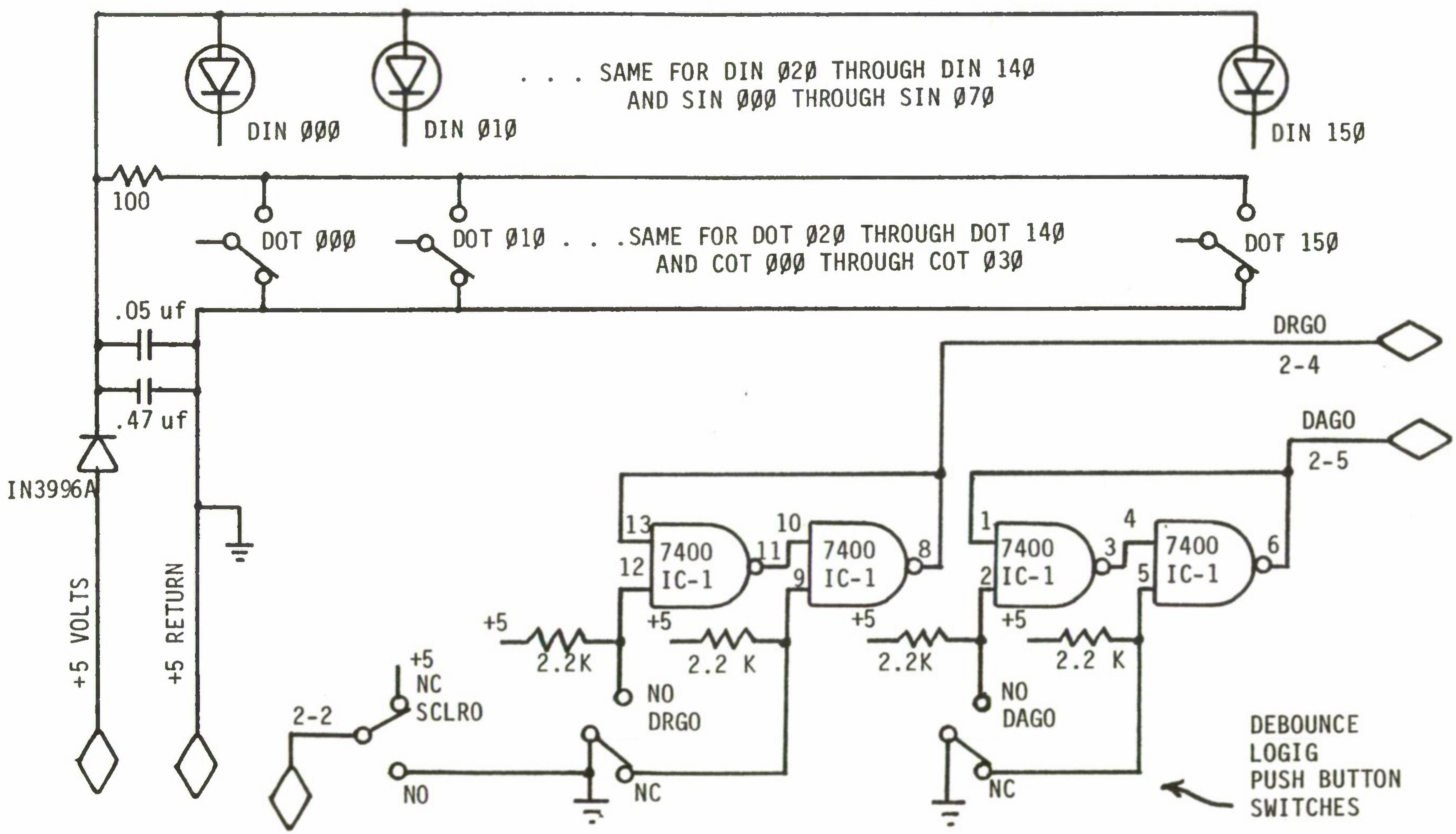



Figure 40. DAU Test Panel Circuit

to replace the sixteen DOT lines, and four COT lines, plus four push button switches to replace the DAGØ, DRGØ, SATNØ and SCLRØ command pulses. Additionally, LED indicators are used to indicate activity on the sixteen DIN lines, the sight SIN lines, and the SATNO line. Debounce logic was used to create clean pulses for DAGØ and DRGØ, as shown in Figure 40. By manually setting the various DOT and COT lines in conjunction with the DAGØ and DRGØ pulses, the DAU can be set up and operated in all modes (see DAU PROBLEM ISOLATION Section II.F.).

## E. DAU ALIGNMENT

### 1. Introduction

Although the majority of the DAU is implemented with digital, LSI, MSI and SSI components, some alignment is necessary on the analog signal path prior to A/D conversion. In a dual channel A/D conversion system such as this, considerable attention must be paid to matching the "inphase" and "quadrature" signal components in order to minimize spectral distortion in the processed spectrum (see Section II.A.2.).

### 2. Theory of Dual Channel Gain Difference

As discussed in Section II.A.2. using dual channel data acquisition allows the use of sample rates in each channel, at one half the rate of single channel data acquisition for the same spectral passband. Dual channel A/D conversion creates complex data points from the "inphase" and "quadrature" analog signal components, thus allowing more efficient use of the discrete fourier transform.

A single frequency sine wave entering the DAU for A/D conversion can be thought of as a rotating vector as shown in Figure 41 (a). The "x" component of the rotating vector represents one channel of signal, while the "y" component represents the other channel of signal. If the gain in both channels from the signal splitter through the A/D converters are not exactly matched, the resultant rotating vector after A/D conversion, will not be circular, but rather elliptical (Figure 41 (b)).

The elliptical vector can be represented by two oppositely rotating vectors of different magnitudes (Figure 41 (c) and (d)), rotating at the same frequency. As an example, consider the vectors in (c) and (d) to be of magnitudes Ø.995 and Ø.ØØ5 respectively. Starting with both vectors pointing in the same direction at position zero, the resultant elliptical vector through one cycle of rotation can be determined. At position zero the sum of both vectors is 1.Ø as shown in Figure 41 (e). At position one, vector (c) is pointing 18Ø degrees out of phase with vector (d) which adds to give resultant vector (e) of Ø.99. Continuing through the cycle the resultant values for positions two and three, as shown by (e), indicates a slightly elliptic vector. This indicates that the resultant spectrum for the resultant elliptic vector could be represented in the fre-

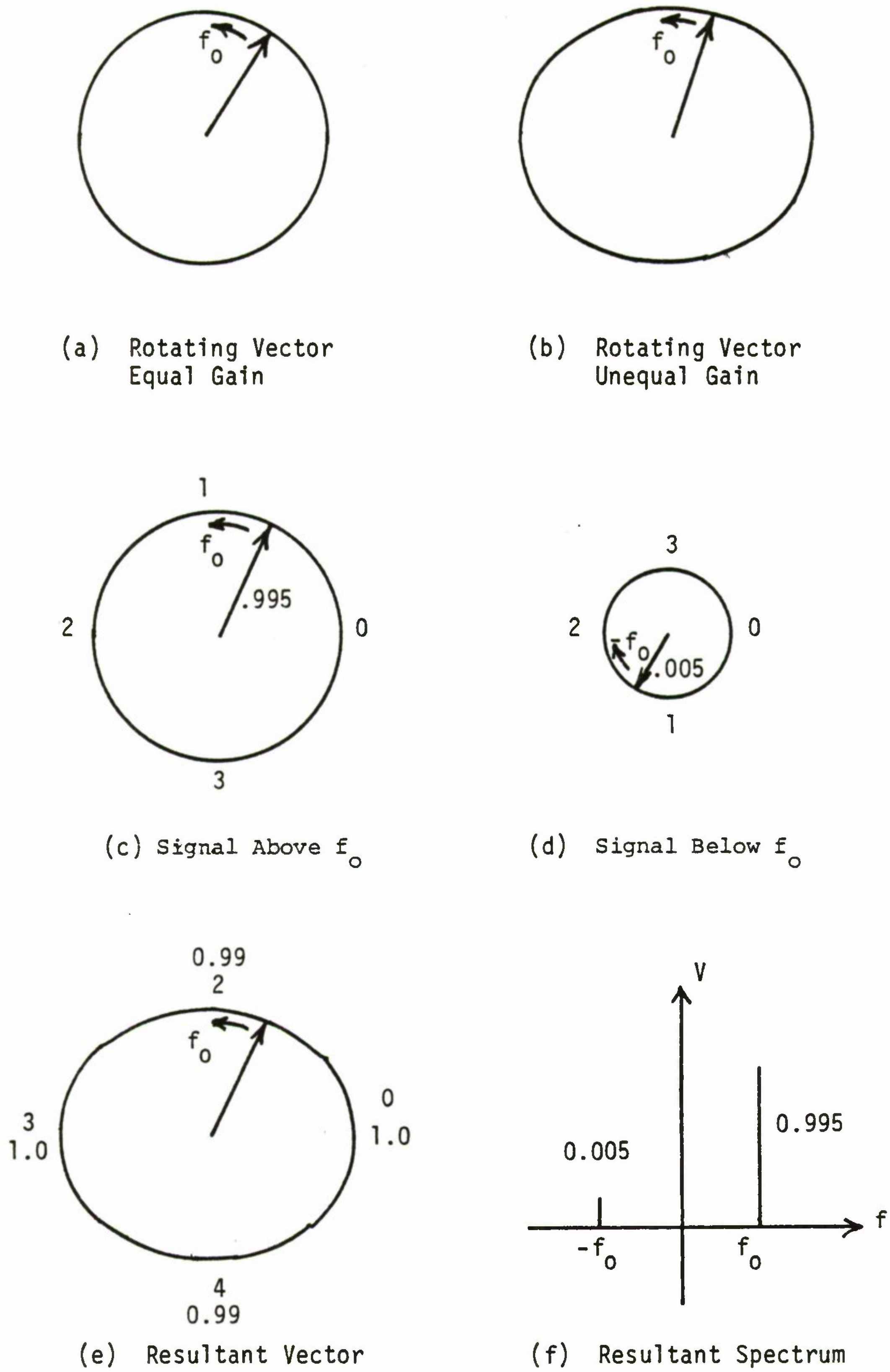



Figure 41. Dual Channel Gain Difference

quency domain by a single major spike at the vector frequency, with a small additional spike occuring at the image frequency (Figure 41(f)). Using the example shown, these two frequency domain spikes would have a voltage ratio of Ø.ØØ5/Ø.995 which is approximately Ø.ØØ5. Then the power ratio is the voltage ratio squared or $2.5 \times 10^{-5}$ which is -46dB.

In addition to the gain error, the amplitude of the image frequency is affected by the phase difference between the "inphase" and "quadrature" signal components, which is determined by the phase difference between the local oscillator signals sent to the baseband mixers (on the high speed ADC boards), and the phase error introduced by amplification and filtering in the two channels. If the phase difference is precisely $90^{\circ}$, then no contribution to the image frequency will occur. If, however the phase difference varies from $90^{\circ}$ by $1^{\circ}$ (as shown in Appendix E) assuming perfect gain alignment, the resultant image frequency will be -35dB, while a $2^{\circ}$ error gives an image frequency of -29.1dB. The phase error from the local oscillator signal can be adjusted to a minimum valve, but the phase error introduced in amplification and filtering cannot be adjusted. Moreover, the amplifier/filtering phase error is a function of frequency, varying as much as $7^{\circ}$ in the low speed channels (due to the Rockland filter). As shown by equation 1 from Appendix E, the relation ship between the gain error and phase error is as follows:

$$\begin{bmatrix}\text{image}\\ \text{signal}\\ \text{component}\end{bmatrix} = \begin{bmatrix}\text{amp/filter} & & \text{L.O.}\\ \text{phase error} & + & \text{phase}\\ & & \text{error}\end{bmatrix}^2 + \begin{bmatrix}\text{gain}\\ \text{error}\end{bmatrix}^2$$

The phase error in the local oscillator signal has been measured and adjusted to a minimum error condition. No further adjustment of this phase difference should be necessary. The amp/filter phase error cannot be adjusted, which leaves only the gain error that must be aligned.

Using this concept, it becomes possible to dynamically align the dual channel acquisition system by inserting a pure sine wave signal at various frequencies through the DAU and then balancing the analog gain in both channels for the minimum image frequency as plotted in the freuqency domain.

3. <u>Static Dual Channel Alignment</u>

a. Introduction

This static alignment procedure is the first step toward achieving a minimum image frequency response from the DAU. Static alignment consists of 1) balancing the analog gain path for the high and low speed paths, and 2) adjusting the sample-and-hold modules and analog-to-digital converter modules for the high and low speed ADC boards.

b. High Speed Static Alignment

To obtain access to the gain trimpots, the High Speed ADC board being adjusted must be put on the 9" wide extender board. Using a variable power supply capable of Ø to ±5 volts and an accurate digital voltmeter, accomplish the following steps in the order given.

(1) Assure a common ground exists between the test equipment and the DAU.

(2) Ground the input of amplifier A1 and adjust trimpot R1 for zero volts (±.Ø1 volts) at the output of amplifier A2. Check that amplifiers A3 and A4 are also close to zero volts.

(3) Set the power supply for a plus 1.28 volts, and apply this to the external input jacks on the front panel via coaxial cable, for both channel inputs. Assure that the front panel switches are in the EXTERNAL position.

(4) Check the voltage at the external input of the High Speed ADC board, edge connector pin 7/11-2-24. Readjust the power supply for 1.278 ±Ø.ØØ2 volts at this point. This step is to overcome the ohmic losses from the front panel to the board and also to try and minimize the voltage variations when the board is installed without the extender board.

For the remainder of the procedure the A/D converters must be sampling at some test rate, preferably 1Ø KHz or 1ØØ KHz to accommodate both high speed and low speed ADC's. This can be accomplished from program control by starting an acquisition while leaving the TEST/NORMAL switch on Control Board (2 of 2) in TEST, or by manually starting an acquisition with the Test Panel (Section II.F.2.) with the TEST/NORMAL switch in TEST. In either case the ADC's are caused to convert continuously. The Test Panel method offers the advantage that both the high and low speed ADC's can be left running by asserting ADC2-HI and ADC2-LO which allows simultaneous alignment of the high speed and low speed analog paths.

(5) Measuring the voltage at the S/H input to the high speed ADC module, pin 17, available as a test point on the upper side of the ADC module, adjust the A2 trimpot, R24, to obtain -1.278 volts ±.ØØ2 volts.

(6) If doing a simultaneous alignment of both the high and low speed analog paths, measure the voltage at the S/H input to the same channels low speed ADC module, pin 32, available at the S/H IN test point, and adjust the A4 trimpot, R25, to obtain -4.995 volts ±.ØØ5 volts. Note that both high and low speed ADC modules receive inverse voltage polarity from the front panel signal due to an odd number of inverting amplifier stages. The low speed S/H module is inverting while the high speed is not. The step up from 1.28 volts to 5.Ø volts between the high speed and low speed ADC modules is provided by gain in A4. Also the low speed ADC board will not have continuity between A4 and the low speed board without the ROCKLAND System 816 filter properly operating.

(7) Reverse the input power supply voltage polarity from plus to minus assureing -1.278 volts ±.ØØ2 volts

available at pin 7/11-2-22. Check the voltage level at the S/H IN test point of the high speed ADC board. If this value is not +1.278 ±.ØØ2 volts the SHM-UH offset gain trimpot must be adjusted. This trimpot, a small screw accessible through a hole in the upper edge of the SHM-UH module, should be set to put the voltage level half way between the plus and minus values.

(8) If doing a simultaneous alignment of both high and low ADC's, measure the voltage at the S/H IN test point on the low speed ADC board. If this value is not +4.995 volts ±.ØØ5 volts adjust the external SHM-5 2Økohm offset, trimpot, located on the low speed ADC board, to put the voltage level half way between the plus and minus values.

(9) Repeat steps (5) through (8) until the analog gain and S/H offset have been set to give the correct full scale bipolar input voltages for the ADC module respectively.

(1Ø) Repeat steps (4) through (9) for the ADC channel not yet aligned. A small amount of voltage variation may occur as a result of removing the board from the extender board. Provided the change is small, the only concern should be in the S/H offset gain adjustments which are accessible from the top of the boards. These adjustments may need to be altered slightly.

c. Low Speed Static Alignment

The low speed ADC alignment can be performed simultaneous with the high speed alignment as discussed in b., or it can be performed separately by following the steps outlined under high speed static alignment that pertain to the low speed ADC boards.

d. High Speed ADC Module Alignment

Independent of the static gain adjustments, the ADC modules themselves need to be adjusted for both gain and offset. The high speed modules, ADC-VH8B2, have four adjustment pots accessible through the inboard side of the modules edge (the screwdriver will be parallel to and just under the RAY-1 mixer module during adjustment). It is most convenient to perform this alignment using the extender board and the ADC module must be operating at some appropriate sample rate (1ØØ KHz can be used for high and low speed modules).

(1) Adjust the power supply, set up as used during the static alignment, to achieve a digital volt meter (DVM) reading at the S/H input test point (above top edge of module) of +1.275 ±.ØØ2 volts DC. With this setting, the parallel 8 bit, two's complement output (at the edge connector pins) should flicker equally between active high 1ØØØØØØØ and 1ØØØØØØ1. This is most easily viewed using an oscilloscope on the least significant bit (LSB, bit 7) making sure that no other low significant bits are high. To achieve this condition, adjust the zero trimpot, the top most pot of the four. Check the adjustment by observing that input voltage +1.27Ø ±.ØØ2 DC, gives 1ØØØØØØ1 steady output, while

+1.28Ø $\pm$.ØØ2 volts DC, gives 1ØØØØØØØ steady output.

Note, the DIN Line LED indicators on the DAU Test Panel (if being used) will give a gross indication of the outputs of both channels simultaneously. If both channels are reasonably close to correct alignment the zero bit, DIN ØØØ, and the seven bit, DIN Ø7Ø, should be the only LED's on.

(2) Reverse the input voltage polarity and set the voltage at the S/H IN test point to -1.265 $\pm$.ØØ2 volts. Adjust the full scale (FS) trimpot, second pot down, output for equal flicker between Ø111111Ø and Ø1111111. Assure that -1.27Ø $\pm$.ØØ2 DC, gives a steady Ø1111111 output.

(3) Repeat steps (1) and (2) until no further adjustment is necessary for the correct outputs on both channels.

e. Low Speed ADC Module Alignment

The low speed ADC modules, ADC-EH12B3, can be easily aligned without the use of the extender board. These modules conveniently provide a serial output port that can be used to observe all 12 output bits on the oscilloscope. This method will not show the two's complement binary output as used in the parallel output port.

(1) Adjust the power supply, set-up as used during static alignment, to achieve a DVM reading of -4.9988 $\pm$.ØØØ2 volts DC, at the S/H IN test point (top center of board). Observing the Serial Out test point (next to S/H IN

test point) on the oscilloscope, adjust the 200 ohm offset trimpot (upper right corner of board) to achieve equal flicker between 0000 0000 0000 and 0000 0000 0001.

Note, the DAU Test Panel will give a gross indication of both channels simultaneously on the DIN 000, MSB, through DIN 150, LSB, LED indicators.

(2) Reverse the input voltage to achieve a DVM reading at S/H IN of +4.9854 ±.0002 volts DC. Adjust the 20 ohm gain pot, upper right corner, to achieve equal, Serial Out, flicker between 1111 1111 1110 and 1111 1111 1111.

Note, the two's complement output as observed on the edge connector pins or on the DAU Test Panel will have zero bit (MSB) inverted. Also, the outputs for the low speed ADC modules is inverted from that of the high speed ADC modules for the same voltage. This is due to the inverting gain of the high speed ADC module. It does not affect the outcome of the spectral plots because of the magnitude squared function of the signal processing.

(3) Repeat steps (1) and (2) until no further adjustment is necessary for the correct outputs of both channels.

4. <u>Dynamic Dual Channel Alignment</u>

a. Introduction

As discussed in Section II.E.2. the final alignment of a dual channel data acquisition system can be performed by minimizing the image frequency response to a single frequency input signal.

b. Dynamic Dual Channel Alignment Procedure

The dynamic alignment procedure must be performed on both the high and low speed ADC boards as outlined in the following steps:

(1) Perform static high and low speed alignment, Section II.E.3.b. and c.

(2) Perform high and low speed ADC alignment, Section II.E.3.d. and e.

(3) Supply a signal near 3Ø MHz to input test point 16 in the Spectrum Receiver, A25. This causes the sinusoid signal to replace the normal receiver output sent to the DAU. This sinusoidal signal will be split in A25 and sent to the high speed ADC board RAY-1 mixers. The difference between the sinusoidal signal and the 3Ø MHz IF quadrature signals will determine the frequency of sinusoidal signal sent to the ADC modules. For example an input of 3Ø.Ø1 MHz would provide a 1Ø KHz signal to the A/D converters.

(4) Adjust the sinusoidal input signal to provide a full scale signal to the A/D converters, approximately -5Ø dBm. Exact full scale level can be obtained by running the A/D converters in the test mode (this will cause the sample-and-hold modules to operate while measuring the AC voltage level at the S/H IN test point on the high or low speed ADC board. Return the TEST/NORM switch to the NORMAL position.

(5) Using the SATCOM spectrum program display

the resulting spectrum for the sinusoidal input on the TEKTRONIX 4Ø14 graphics display console using a log plot (i.e. operate this program normally setting program parameters as appropriate for the input signal). The resulting spectrum should show a pair of spectral spikes at the frequency and image frequency of the input signal. The object of the alignment is to cause the image frequency spike to be suppressed greater than 25 dB for the high and low speed ADC operation.

(6) If the image frequency is not low enough, cause the DAU to operate in the TEST mode and adjust the high speed S/H IN test points on both high speed boards for identical AC voltage values using trimpot R23 (located in the feedback loop of A1 on the high speed ADC board). This adjustment is possible to do without using the extender board.

(7) Return TEST/NORMAL switch to normal and obtain spectrum results. If the result is still not 4Ø dB of image frequency suppression, adjustment of the IF local oscillator signal supplying the channel 1 and channel 2 mixers may need to be aligned for perfect quadrature. To adjust for quadrature first assure that the X-Y plot of the input signal looks like a circle at the HP-122Ø oscilloscope. Next add an elbow BNC connector to the input calbe of jack J26 in receiver A25. This will alter the LO signal phase by the increment associated with the length of signal path added by the BNC connector. Add or subtract connectors in this manner to achieve the required high speed alignment.

(8) Remember that adjustment of the high speed amplifier chain affects the low speed gain. Repeat steps (5) and (6) to achieve dynamic alignment of the low speed channel; however, trimpot R25 in the feedback loop of A4 on the high speed ADC board must be used for gain adjustment of low speed ADC's. Adjustment of R25 will not affect the high speed alignment. Do not readjust the LO quadrature phase as per step (7). R25 can only be adjusted by using the extender board. Check the spectral output in this step while the high speed board is both on and off of the extender board. Greater than 5Ø db of image frequency suppression should be achieved for the low speed A/D converters.

F. PROBLEM ISOLATION

1. Introduction

Problem isolation for the DAU can be quickly isolated to a suspect area by inspection of the various LED indicators, visible from the top of the DAU, and use of the various easily available test points. An understanding of the basic DAU operation in each of its possible modes will be necessary before trouble isolation can continue. Use of this report, Chapter II, should enable anyone, technician or student, to isolate any given problem on both a macro and micro level. Section headings throughout this report have been specifically chosen to allow its use as a look up device for specific questions, without unnecessary reading of lengthy descriptions.

The DAU Block Diagram, Figure 3 should serve as a quick reference to suspect areas, and hence lead to the correct operational description.

2. <u>Use of DAU Test Panel</u>

a. Introduction

As discussed in Section II.D. the DAU Test Panel is a device capable of replacing the INTERDATA 7/32, relative to the DAU, thereby allowing manual control of the DAU at human speeds. Operation of the DAU for each of its modes is discussed below.

b. Test Panel Operation for Mode I

Mode 1, or the acquisition mode, can be set up as follows. The order of listed steps is compatible with the software control sequence.

(1) Replace INTERDATA 7/32 cables II and III at the DAU backplane with cables II and III from the DAU Test Panel. Assure that the +5 volt power leads for the Test Panel are connected to an operational power supply.

(2) Connect a coaxial cable (5Ø ohm) between the Syntest Output jack (located near the ADC Protect board) and a counter to indicate SM-1Ø1 activity.

(3) On the front of the test panel set COT switches (up position for 1) to hexidecimal 1 (ØØØ1 binary). Set DOT switches to hexidecimal ØØØ6 (ØØØØ ØØØØ ØØØØ Ø11Ø binary). Push DAGØ. This has loaded the RANGE register (Control Board (2 of 2) for SM-1Ø1 operation in the 1ØØ KHz range.

(4) Set COT switches to hexidecimal 2 (ØØ1Ø binary). Set DOT switches to hexidecimal 1ØØØ (ØØØ1 ØØØØ ØØØØ ØØØØ binary). Push DAGØ. This has loaded the FREQUENCY register for SM-1Ø1 frequency of 1ØØ KHz which should be indicated by the counter.

(5) Set COT switches to hexadecimal 3. Set DOT switches to hexadecimal Ø4ØØ. Push DAGØ. This has set the word count (WC) register to 1Ø24.

(6) Set COT switches to hexadecimal 4. Set DOT switches to hexadecimal ØØØØ. Push DAGØ. This has set the address register (ADD) to starting address of zero.

(7) Set COT switches to hexadecimal 5. Set DOT switches to ØØ11. Push DAGØ. This has set the CONTROL register to ADC2-LO and ADC-LO to start a low speed ADC acquisition for a block size of 1Ø24 and sample rate of 1ØØ KHz. The acquisition will have occurred so fast as to be barely visible. By watching the BUSY Ø status light (SIN Ø4Ø) or the SATNO light, the acquisition will appear as a blink of the LED. Note the CONTROL register LED indicators located along the top of Control Board (2 of 2), are arranged in the same order as DOT switches required to set them (i.e., COT switches to hex 5 and DOT switches to hex ØØ11 has turned on ADC2-LO and ADC-LO, while DOT ØØ22 would turn on ADC2-HI and ADC-HI).

(8) To start an acquisition without allowing the WC register to reset the DAU and terminate the acquisition, the TEST/NORM switch on Control Board (2 of 2) should be placed in the TEST position. Then repeat steps (3) through (7). The DAU will now be continuously acquiring data through the low speed converters at a 1ØØ KHz rate. In this condition the SIN Ø4Ø LED should stay on while the SATNO LED remains off, indicating a busy DAU. EOC signals for the low speed converters and EOCM and SSYNCBO should all be active signals observable with an oscilloscope at the test points available along the top of the Buffer Memory Timing board. Switching the TEST/NORM switch to NORM will terminate the acquisition when WC goes to zero.

c. Test Panel Operation for Mode II

Mode II, or data transfer from DAU buffer memory to the INTERDAT 7.32, can be simulated by the following steps.

(1) Follow steps (1) through (6) of Mode I Test Panel Operation. Step (3) and (4) are unnecessary and can be omitted if desired.

(2) Set COT switches to hex 5. Set DOT switches to hex ØØØ4. Push DAGØ. Now each time DRGØ switch is pushed the DIN LED indicators will read the data (left justified) stored in buffer memory for first channel 1 and then channel 2 for each address location starting at address zero. Note that the DIAL output must be pushed twice to force out old data and load the first word of good data.

d. Test Panel Operation for Mode III

Mode III, or the diagnostic data transfer mode, can be simulated by the following steps:

(1) Follow steps (1) through (6) of Mode I Test Panel Operation. Steps (3) and (4) may be omitted if desired.

(2) Set COT switches to hex 5. Set DOT switches to hex ØØØ8. Push DAGØ.

(3) Set COT switches to hex Ø. Now each time the DAGØ switch is pushed the data values set by the DOT switches (left justified) will be stored in buffer memory starting with channel 1 at address zero.

e. Summary

By the logical application of the DAU Test Panel the DAU can be manually programmed to perform anything within its capability. The specific switch settings for the DOT switches as listed above are just examples for possible use. Any variations can only affect the SM-1Ø1 frequency and the WC and ADD registers to perform as desired.

One simple example of Test Panel use might be to load (Mode III) ten specific memory locations with a particular data pattern and then read out (Mode II) those locations. This test, although simple, tests everything in the DAU except the ADC board and the ADC Timing Board. Properly operated the DAU Test Panel becomes perhaps the most effective tool for DAU problem isolation.

f. Quick Reference Charts

To obtain quick reference to the DAU operational aids, refer to Tables II and III. Table II lists the function associated with each DAU internal LED indicator, test point and switch and tells whether a lighted LED is for an active high or active low level, and what each test point and switch is for. Table III provides a quick reminder of how to control each mode of the DAU with the DAU Test Panel. The numbers listed in the table do not refer to the bit numbers scribed above the switches, but rather, they refer to hexadecimal numbers for groups of four switches.

TABLE VIII - DAU INTERNAL PROBLEM ISOLATION AIDS (Page 1 of 3)

| Location | Signal | LED | Active Level for Light on | Test Point Available | Switches | Comments |
|---|---|---|---|---|---|---|
| Control (1 of 2) Board 8 | SATNO | Yes | Low | Yes | ---- | DAU request attention |
| | BUSYØ (SIN Ø4Ø) | Yes | Low | Yes | ---- | DAU unavailable to 7/32 |
| | OVO (SIN Ø5Ø) | Yes | Low | Yes | ---- | ADC over-run |
| | EOM (SIN Ø6Ø) | Yes | Low | Yes | ---- | WC = 0 with transfer pending |
| Control (2 of 2) Board 10 | ADC-LO | Yes | High | No | ---- | Low speed acquisition Mode I |
| | ADC-HI | Yes | High | No | ---- | High speed acquisition |
| | 7/32 RD | Yes | High | No | ---- | Transfer data to 7/32 Mode II |
| | 7/32 WR | Yes | High | No | ---- | Transfer data from 7/32 Mode III |
| | ADC2-LO | Yes | High | No | ---- | Low speed prestart |
| | ADC2-HI | Yes | High | No | ---- | High speed prestart |
| | M/M WC | No | Low | No | TEST/ NORMAL | Test prevents WC = 0 |
| High Speed ADC Board 7/11 | S/H IN | No | --- | Yes | ---- | S/H input to ADC module |

TABLE VIII - DAU INTERNAL PROBLEM ISOLATION AIDS (Page 2 of 3)

| Location | Signal | LED | Active Level for Light on | Test Point Available | Switches | Comments |
|---|---|---|---|---|---|---|
| Low Speed ADC Board 5/13 | S/H IN | No | --- | Yes | ---- | S/H input to ADC module |
| | SERIAL OUT | No | --- | Yes | --- | Serial out of ADC module |
| Buffer Memory Timing Circuit Board 16 | EOC-LO CHN 1 | No | Low | Yes | ---- | Mode I only |
| | EOC-LO CHN 2 | No | Low | Yes | ---- | Mode I only |
| | EOC-HI CHN 1 | No | Low | Yes | ---- | Mode I only |
| | EOC-LO CHN 2 | No | Low | Yes | ---- | Mode I only |
| | EOCM | No | Low | Yes | ---- | Mode I only |
| | SSYNCBØ | No | Low | Yes | ---- | Mode I only |
| ADC Protect Aux 4 | P4, +24 | Yes | +24 | No | ---- | To SM-101 |
| | P5, +10 | Yes | +10 | No | ---- | To SM-101 |
| | P16, +5 | Yes | +5 | No | ---- | Main logic |
| | P17, -5 | Yes | -5 | No | ---- | CH1, CH2 ADC bds |

TABLE VIII - DAU INTERNAL PROBLEM ISOLATION AIDS (Page 3 of 3)

| Location | Signal | LED | Active Level for Light on | Test Point Available | Switches | Comments |
|---|---|---|---|---|---|---|
| ADC Protect Aux 4 (cont.) | P18, +15 | Yes | +15 | No | ---- | CH1 ADC bds |
| | P18, -15 | Yes | -15 | No | --- | CH1 ADC bds |
| | P19, +15 | Yes | +15 | No | ---- | CH2 ADC bds |
| | P19, -15 | Yes | -15 | No | ---- | CH2 ADC bds |
| | P20, +5 | Yes | +5 | No | ---- | CH1 ADC bds |
| | P21, +5 | Yes | +5 | No | ---- | CH2 ADC bds |
| Front Panel | PWROK | Yes | Low | No | ---- | All power supplies on |

TABLE IX - DAU TEST PANEL OPERATION

| Mode | COT Switches | DOT Switches | DAGO Switch | Comments |
|---|---|---|---|---|
| | 1 | 0006* | X | Range register 1ØØ kHz |
| | 2 | 1000* | X | Frequency register |
| | 3 | 0400* | X | WC register, 1Ø24 |
| I | 4 | 0000* | X | ADD register, zero |
| | | 0020 | X | High Speed Acquisition |
| | 5 | 0011 | X | Low Speed Acquisition |
| | | 0030 | X | Low and High Speed ADC's on |
| | 3 | 0040* | X | WC register, 1024 |
| II | 4 | 0000* | X | ADD register, zero |
| | 5 | 0040 | X | 7/32 RD |
| | 3 | 0400* | X | WC register, 1024 |
| III | 4 | 0000* | X | ADD register, zero |
| | 5 | 0008 | X | 7/32 WR |

* Example values shown

# III. SATCOM SIGNAL ANALYSIS SOFTWARE

## A. GENERAL INFORMATION

### 1. Introduction

After the Data Acquisition Unit (DAU) was made operational, and the interface software programs were written /Ref. 14/, A program was required to exercise the DAU within the SATCOM Signal Analyzer System. This program, written in FORTRAN V for the INTERDATA 7/32, would need to cause the DAU to acquire data at the correct sample rate and block size, pass the data to the INTERDATA 7/32, further pass the data to the AP-12ØB Array Processor, direct the data processing in the SP-12ØB, receive the resultant data back from the AP-12ØB and finally direct the TEKTRONIX 4Ø14 Graphics Display Terminal to plot the resultant signal spectrum. An overview of the program that performs the stated requirements is discussed below. This program has been named SATCOM and will be referred to as such throughout.

### 2. SATCOM Spectrum Analyzer Programming Objectives

#### a. Introduction

The SATCOM (spectrum analyzer) program is designed to meet five basic objectives required for processing time domain data from the DAU into frequency domain spectral output. The five basic objectives for SATCOM are: 1) initialization, 2) control, 3) data acquisition, 4) computation, and 5) display. The combination of these objectives as specified by the SATCOM program, integrates a large amount of laboratory assets into a total SATCOM Signal Analyzer capable of performance unobtainable with the standard analog spectrum analyzer.

b. Initialization

Default values for all necessary program parameters are specified in the initialization section of the program. This allows that limited spectral analysis is possible by default, i.e., no external control parameters.

c. Control

Under the control section of the program a complete set of operating parameters from the system operator are specified utilizing an interactive portion of software and the INTERDATA 7/32 keyboard terminal. This is accomplished by the program asking the operator for answers to a set of questions. With the answers, the INTERDATA can set up all necessary hardware to perform the spectral analysis. This interactive programming will ultimately take place between the control panels [Ref. 1] and the SATCOM program to allow a more convenient method for system operation.

d. Data Acquisition

Data Acquisition is obtained via the DAU through INTERDATA 7/32 commands as articulated in this portion of the SATCOM program. By using FORTRAN V CALL statements to a DAU support program library (DAUSUP.OBJ) [Ref. 1], data acquisition parameters are set up, data obtained, and then DMA-transferred to the INTERDATA. This step can be repeated several times when averaging more than one block of data before displaying the result.

e. Computation

All mathematic computation is performed by the AP-12ØB Array Processor using software programs supplied as part of the AP-12ØB package /Ref. 12/. In the computation portion of SATCOM, the DAU data is DMA transferred to the AP-12ØB, and operated on in the AP using FORTRAN V CALL statements to access the AP support library (APSUP.OBJ) under INTERDATA control. Upon completion of data processing the resulting data is transferred (DMA) back to the INTERDATA for display. When processing more than one block of data, the DAU data is fed to the AP for processing where the averaged result remains until the last block of data is processed.

f. Display

The final signal spectrum is displayed on the TEKTRONIX 4Ø14 (GDT) Graphics Display Terminal /Ref. 14/. Scaling and formatting of resultant data is performed by the software routines included as part of the TEKTRONIX 4Ø14 package, using FORTRAN V CALL statements. Scaled and formatted data is then transferred via TTY interface to the GDT and displayed on a storage type CRT. Hard copy of the GDT display is available via TEXTRONIX's 4631 hard copy unit /Ref. 14/. Resultant spectrum plots are available as full scale single plots, or can be displayed in three dimensions, with the time access proceeding apparently into the screen. In this operational mode, data acquisition, computation and display are repeatedly performed.

3. Use of the FLOATING POINT SYSTEMS AP-12ØB Array Processor

a. Introduction

The Floating Point System AP-12ØB Array Processor is a high speed dedicated processor built specifically to perform computation bound algorithms on streams, or arrays, of data. In contrast with the INTERDATA 7/32, the AP-12ØB contains no provision for dynamic interupt handling and no executive software resides in the AP-12ØB. The AP-12ØB is programmed by the INTERDATA 7/32 upon request of the operating program in the 7/32. Data passed to the AP-120B is processed by the program passed to the AP-12ØB and upon completion the resultant data is passed back to the requesting program. In this way, the AP-12ØB is an I/O peripheral device like any other as far as the 7/32 executive program is concerned. When viewed from the user's standpoint, writing programs in FORTRAN, the AP-12ØB appears to be something like a scientific subroutine package, with no direct indication that a special hardware device is being accessed. All of the programming necessary to achieve the interface between the FORTRAN CALL statements and the actual running of the AP-12ØB has been supplied by Floating Point Systems, including an extensive library of FORTRAN callable subroutines. Additionally, programs specific to the user's demands can be written in AP-12ØB microcode and included as part of the AP library.

The AP-12ØB achieves an incredible speed factor over the general purpose minicomputer by taking advantage of signal processing algorithms and providing parallel data paths for various functions internal to the AP-12ØB. The AP-12ØB in addition to the parallel data paths, uses a "pipelining" technique to further speed up processing. Pipelining is a technique whereby operations are performed in several stages with data actively being processed in each stage simultaneously. For example, floating point multiplication is broken into three stages consisting of two stages generating products of fractions and a last stage consisting of adding exponents and normalizing. For any one isolated multiplication, three cycle times would be required to obtain the result; however, for large arrays of data a multiplication every cycle with the output delayed three cycles from the input (a small amount of overhead is required to fill the pipeline and empty it at the end). Further information concerning the AP-12ØB is available in Reference 12. By using the AP-12ØB in the SATCOM signal analyzer system, signal processing at rates comparable to large mainframe systems is possible while using a minicomputer system such as the INTERDATA 7/32.

b. Using FORTRAN Callable Subroutines

Use of the AP-12ØB in the SATCOM program is done entirely by programs available in the AP support library. To utilize an available AP program requires only that correct parameters be passed in the CALL statement as defined by Reference 12, AP Math Handbook, and that data is available in AP-12ØB main memory as specified at the time of the CALL. The AP-12ØB in this installation contains 768,64 bit words of program source (PS) random access memory (RAM). At the time of the CALL statement in the INTERDATA program a search of the AP-12ØB PS memory is initiated. If the program called for is not already stored in the PS memory, the INTERDATA transfers that program into the PS memory and then the program is executed. Programs are stored in PS memory on a last in, first out (LIFO) basis. Thus, if the most lengthy and important programs are stored in the top of PS memory, they will remain resident in the AP and the CALL statement will only start the program without the overhead of transferring the program to the AP at the time of each call. The number of PS memory locations required for each AP program is listed in the AP-Math Handbook. For the SATCOM program, 768 words can contain all of the needed AP programs. If this were not the case, it might be more efficient to perform a "dummy" set of AP CALL's to store the longest and most often used programs at the top of PS memory. The AP12ØB configuration for this installation is included in Appendix 2.

c. Use of AP-12ØB Wait States for Data Transfer

All data passed to or from the AP-12ØB is done so via a DMA port with INTERDATA. The DMA transfer of data is initiated by an APPUT,CALL statement (transfer to the AP) or an APGET,CALL statement (transfer from the AP). If the program steps following an APPUT call are data processing calls, an APWD (AP wait data), CALL must be inserted to assure that the AP does not process the follow up statements before the data has completely arrived. Likewise an APWR (AP wait results) is used to assure that the AP computations are complete before the APGET transfer is initiated. If the data can be guaranteed to be at the location specified in the AP before the processing routines are called, then the wait states can be omitted. This fact is used in the SATCOM program to initiate an APPUT to one location in AP memory while all subsequent processing calls are made to a location that was filled in a previous APPUT. In this manner, maximum efficiency can be made of the AP's speed and DMA capability with processing and data transfer toggling between memory locations simultaneously.

d. Efficient Use of AP-12ØB Memory

The AP-12ØB main data memory, for this installation, (MD) is built with MOS semiconductor RAM chips that require 333 nanoseconds of access time. This is two AP cycle times (the AP runs at 6 MHz which is 167 nanosecond cycle time). In order to allow the MD memory to be accessed once per cycle, the AP memory is designed to "interleave" between 4 K blocks of memory. Addressing a vector sequentially (Ø1234 . . .) physically stores the even addresses in the first 4 K block of memory and the odd addresses in the second 4K block of memory. Therefore addressing a vector sequentially allows maximum memory access provided the vector operation being performed does not require two accesses from the same block of memory. The SATCOM program was organized to take advantage of the most efficient use of AP memory.

4. Use of the TEKTRONIX 4Ø14 Graphics Display Terminal

a. Introduction

The TEKTRONIX 4Ø14 Graphics Display Terminal (GDT) combined with the Terminal Control System (TCS) Software Library (also called the PLOT 1Ø package) makes up a subsystem within the SATCOM Signal Analyzer System. In the specific case of the SATCOM program this subsystem provides the capability of changing an array of resultant data into a meaningful plot that will remain on a storage CRT (the 4Ø14 terminal) for short term analysis, or that can be permanently copied on the TEKTRONIX 4631 Hardcopy Unit.

b. Use of FORTRAN Callable Subroutines

In the same way that the AP-12ØB is accessed from a user FORTRAN program, the GDT can be accessed, using FORTRAN CALL statements to specific programs that are a part of the TCS library. The TCS library includes programs for moving the GDT cursor, drawing connecting lines between two points, scaling the data for proper screen fit, writing screen alphanumerics and a host of other programs. In each case the subroutines are utilized through a FORTRAN CALL statement and the proper passing parameters. Further information on using this portion of the system can be obtained from Reference [13].

c. Modified TCS Subroutine

One of the TCS subroutines that deals with alphanumeric strings to be plotted on the screen, has been used in a modified form to facilitate easier plot labeling from the user program. The Plot 1Ø subroutine ANSTR is used within a subroutine called ANBSTR written in assembly language and included in the SATCOM program. Use of this subroutine is explained in the comments of SATCOM.

d. GDT Resolution

The GDT is capable of plotting in two different resolutions, either a 1Ø24 x 1Ø24 resolution or a 4Ø96 x 4Ø96 resolution as specified. The 4Ø96 x 4Ø96 resolution is used throughout the SATCOM program.

5. <u>Programming Philosophy</u>

a. Readability

The SATCOM program was built using the top down approach to programming. The basic objectives were defined, and organized as major subroutines. Then the main program was written to perform a simple less than optimum efficiency spectrum making references to the major subroutines. Next the major subroutines were written by defining what each to accomplish and forming any reasonably extensive code into additional subroutines. In this manner the five major objectives were met with a program more concerned with user readability than efficiency and minimum program size.

b. Efficiency

After a program was built that could perform basic spectrum analysis on a single block of data, the program was modified to allow block averaging of processed data to be done in as efficient a manner as possible, relative to the AP-12ØB. The efficiency was achieved primarily by transferring data into an alternate section of AP-12ØB MD memory while processing on data stored in a previous iteration. Additionally, the DAU data was maintained in integer form until it was processed by the AP-12ØB. Table X lists software Do's and Don'ts applicable to the SATCOM Signal Analyzer.

B. GENERAL SATCOM DESCRIPTION

The SATCOM program is shown in flow chart form in Figure 42 and Figure 43. Figure 42 shows the main portion of the programspecifying the significant options exercised there. If only one output plot is desired, subroutine BLOCKS is called to acquire data in the specified size of blocks, the data is processed to produce the Fourier Transformed spectrum of the signal, and if more than one block is to be averaged, the process is repeated. Figure 43 shows a flow chart of subroutine BLOCKS indicating the efficient use of DMA data

TABLE X - SOFTWARE DO'S AND DON'TS FOR PROPER DAU OPERATION (Page 1 of 2)

This table suggests some possible do's and don'ts applicable to the SATCOM Spectrum Analysis Program or future versions of DAU controlling programs. The major objective of these suggestions is to increase signal throughput while assuring proper DAU operation.

DO'S

1. Assure that the desired sample rate is loaded into the DAU (CALL BCDFREQ) prior to at least 1ØØ milliseconds of program delay before starting the DAU in an acquisition mode (CALL ACQUIR). This allows adequate time for the SYN-TEST Frequency Synthesizer to stabilize at its new frequency.

2. Cause the DAU Prestart Circuit to be started for the appropriate A/D converter prior to starting the acquisition. This is done by loading the DAU control register with a high on DOT 1ØØ or DOT 11Ø for ADC2-HI or ADC2-LO respectively. This starts the A/D converter and allows the Prestart time out prior to data acquisition. This bit does not need to be changed again until the spectrum requirement dictates a change to the alternate (high or low) A/D converter. Each block of data acquisition need only be initiated by asserting ADC-HI or ADC-LO, accomplished by asserting high DCT 14Ø or DOT 15Ø respectively, on the DAU control register.

TABLE X - SOFTWARE DO'S AND DON'TS FOR PROPER DAU OPERATION (Page 2 of 2)

DON'TS

1. When causing acquisition to be taken with the alternate set of A/D converters, do not change DOT 1ØØ and DOT 11Ø, ADC2-HI and ADC2-LO on the DAU control register in the same program step. It must be done in two step (i.e., the asserted bit brought low in one step and then the alternate bit asserted high in the next program step). This assures that the DAU Prestart Circuit can reset to allow the prestart sequence to commence for the desired A/D converters. Failure to do this can cause the majority of the first block of acquisition to contain bad data.

2. When loading the DAU control registers, loading in sequence registers one through five will assure proper DAU operation. Variations of that sequence could cause improper operation. Do not load register five before registers one through four have been properly loaded unless just loading ADC2-LO/HI. ADC2-LO/HI does not start an acquisition but only prestarts the A/D converters.

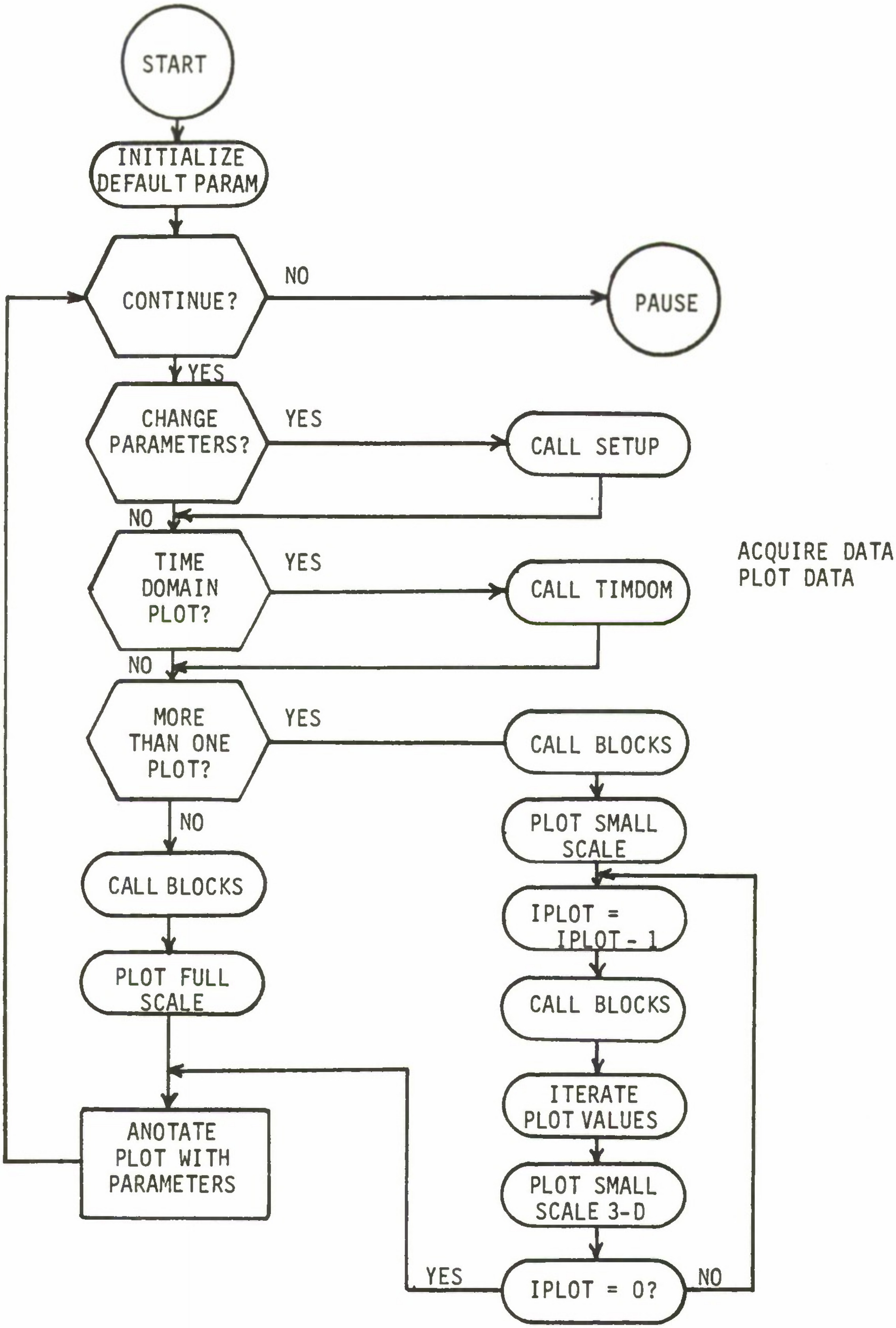



Figure 42. SATCOM Program (Main Routine)

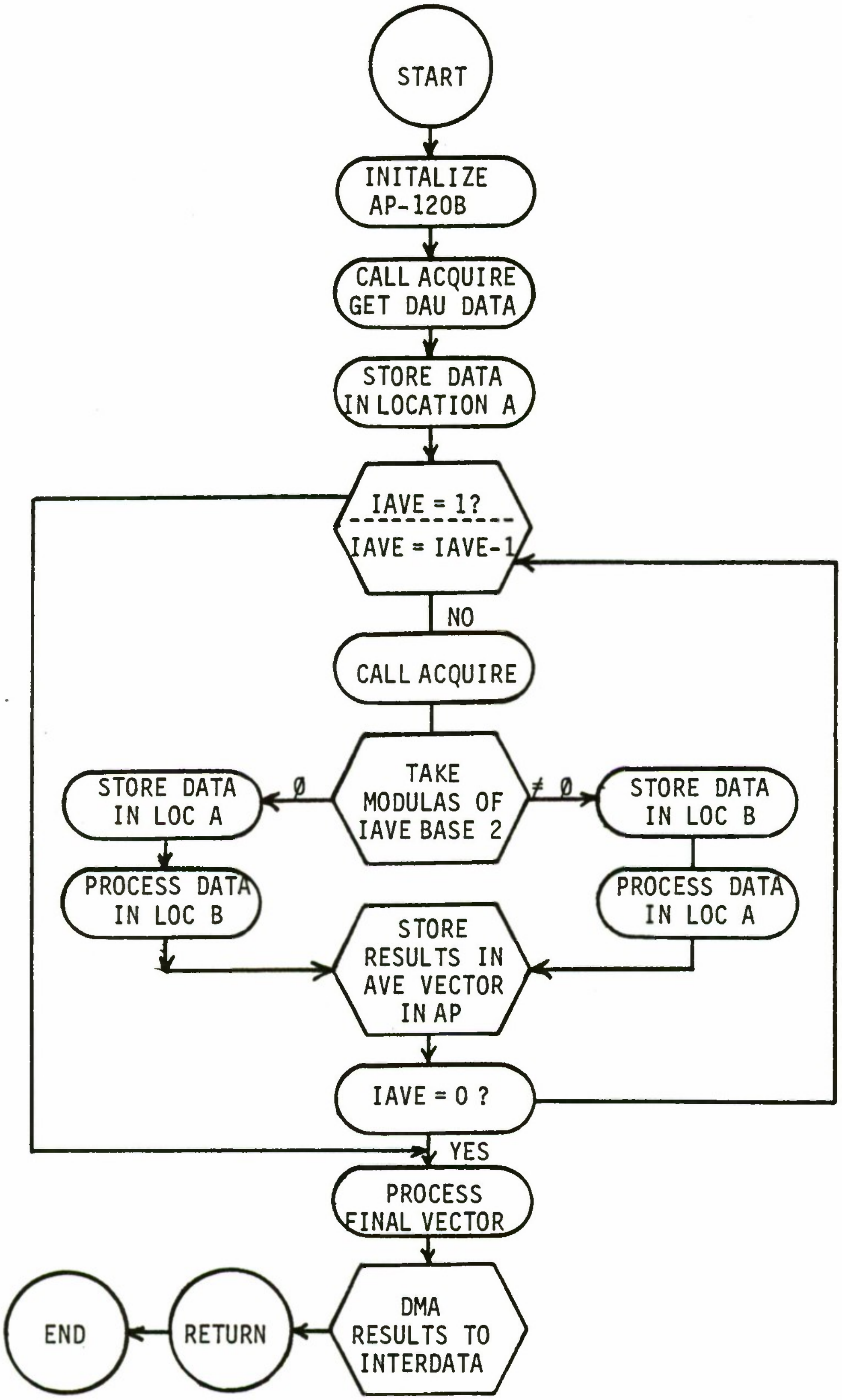



Figure 43. SATCOM Program, BLOCKS Subroutine

to the AP-12ØB by a toggling technique. Subroutine BLOCKS returns resultant data that is plotted as necessary by several subroutines dedicated to the plotted presentation.

If more than one output plot is to be presented to a three dimensional fashion, the main program loops back around through subroutine BLOCKS for as many plots as specified, plotting each successive plot above and to the right of the previous plot. Figure 44 shows an example of the full scale single plot and Figure 45 shows as example of the multiplot 3-d output.

This program represents a simplified first version usage of the SATCOM Signal Analyzer System. Follow-on versions will be generated and integrated into the remaining hardware to complete the operational system. Table X suggests some necessary do's and don'ts for SATCOM Signal Analysis software.

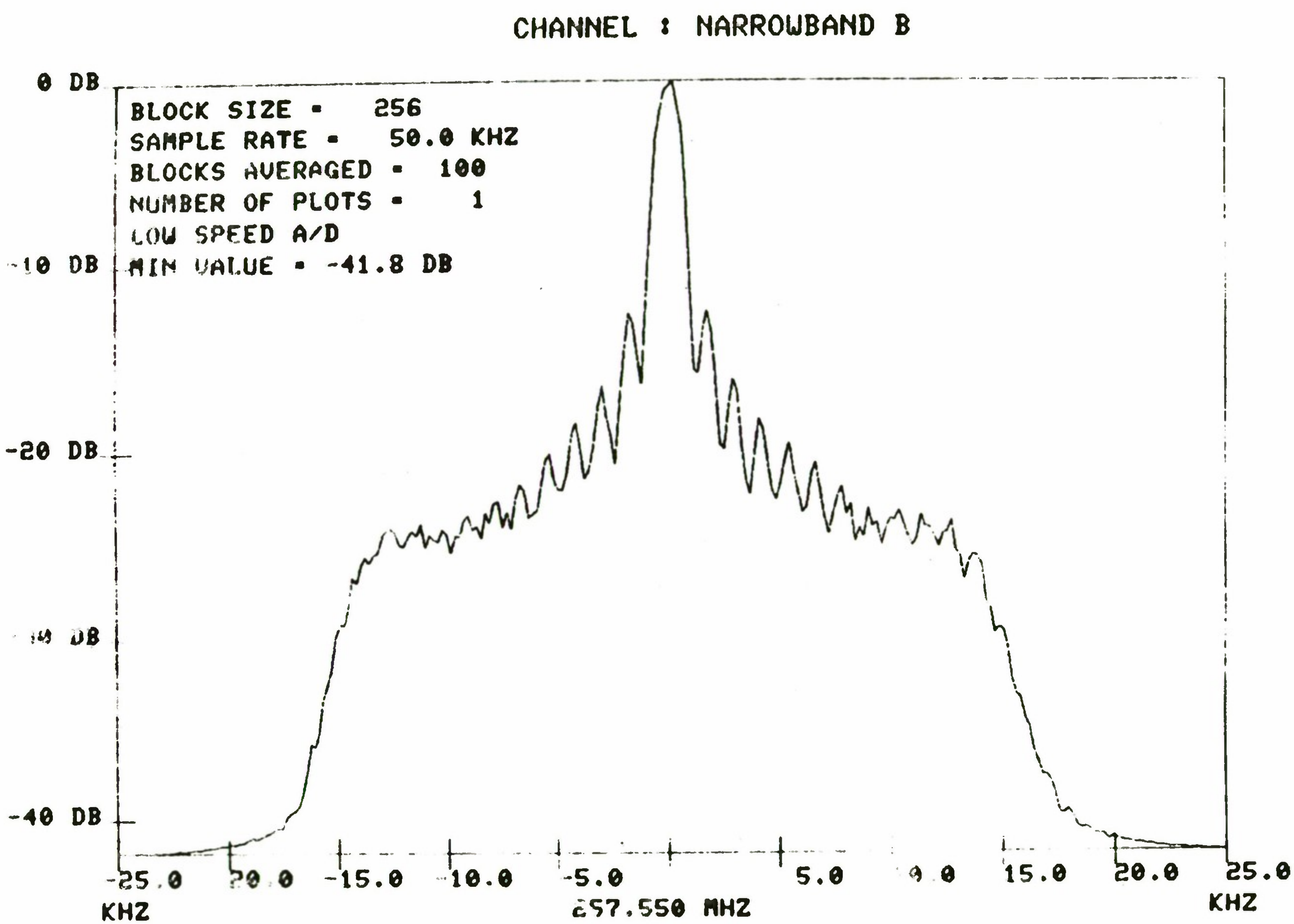



Figure 44 - SATCOM Single Plot Example

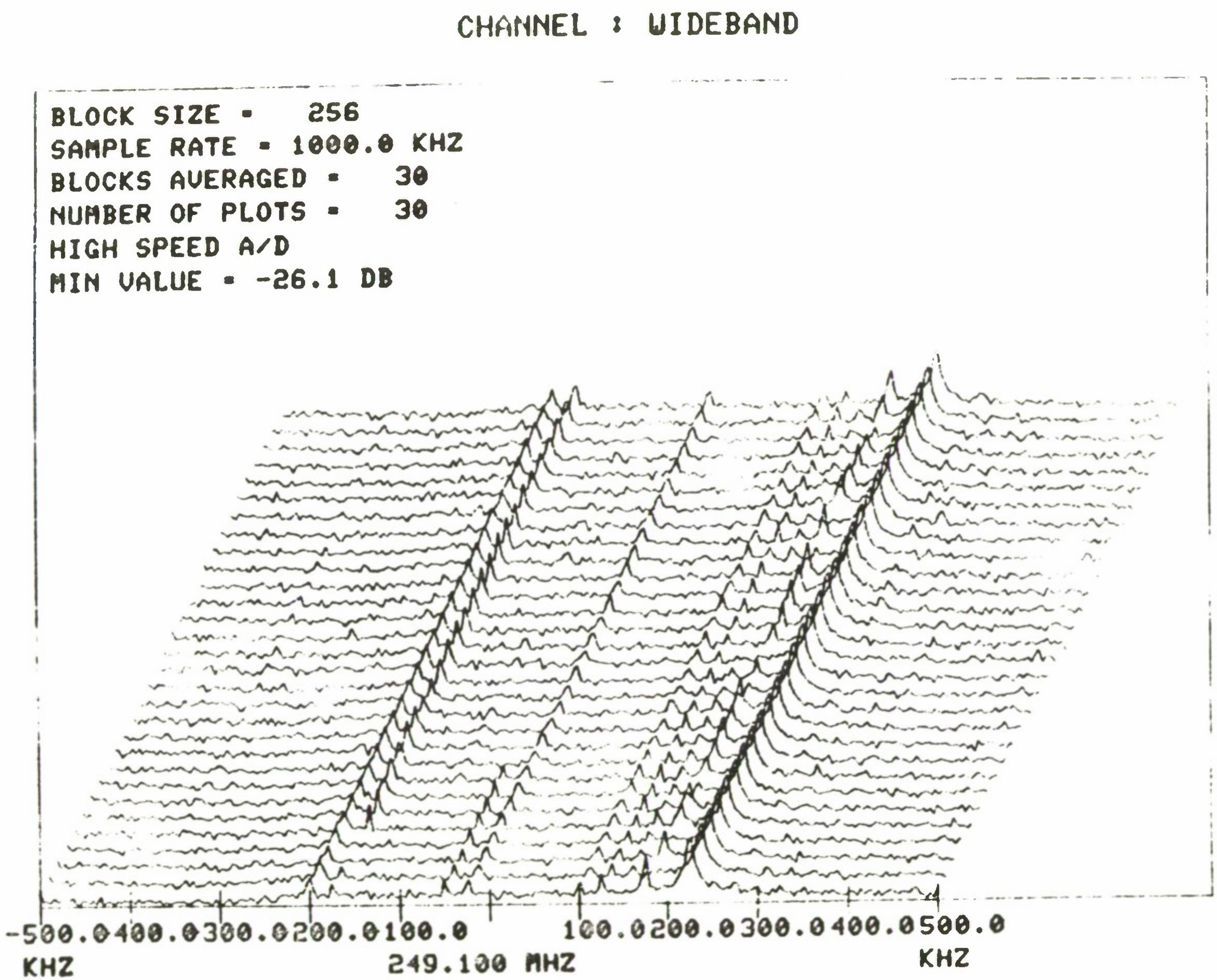



Figure 45 - SATCOM Multiple Plot Example

## IV. OPERATIONAL PERFORMANCE CHARACTERISTICS

### A. INTRODUCTION

Although the SATCOM Signal Analyzer has not yet become an operational system some comments can be made concerning its performance characteristics. The DAU was designed to handle a frequency bandwidth capable of displaying the entire bandwidth of the satellite signal being observed. Also the rate at which spectral information can be obtained, or throughput, should be as close to real time analysis as possible. More important than throughput, is the accuracy with which the spectrum has been produced using the discrete Fourier Transform method. These and related items are discussed in the following sections.

### B. FREQUENCY RESOLUTION AND BANDWIDTH

The Discrete Fourier Transform (DFT) can only approximate the results of a true mathematical Fourier Transform due to the finite and discrete properties inherent in it. The results of the DFT can be thought of as a bank of bandpass filters each covering a slightly different band, with N of these BP filters making up the entire transform bandwidth. The bandpass filters overlap each other at their 4dB points at which point they have individual bandwidths of 1/T where T is the period of the assumed repetition of the Fourier Transform. For the discrete case T is the period of the sample block, or N times d where N is the number of samples in a block and d is the period of the sample frequency. For dual channel A/D conversion, if the sample rate is fixed (i.e., d is fixed) then the frequency band covered unambiguously is 1/d for any value of N. It follows that :

$1/d = BW$

or sample rate $= f = BW$

also $T = Nd$

then $1/T = \frac{1}{Nd}$

if N increases with fixed d, 1/T decreases,

or if N decreases 1/T increases.

Therefore, the bandwidth of the individual filters that make up the spectral bandwidth vary with N. The result of the DFT is accurate at multiple of 1/T or where the spectral component occurs at the peak of a specific individual filter. Any frequency component that is not a multiple of 1/T then occurs somewhere along the skirt of the filter down to the 4dB point where it starts falling within the bandpass of the adjacent filter. This inaccuracy is called the "picket fence error", so named due to its resemblance of a picket fence. If it were allowable to sample forever and then perform, a DFT the 1/T bandwidth would become so small as to be negligible. However, in this particular implementation the maximum number of samples per block, N, is 2048 corresponding to the size of the buffer memory. The highest sample rate that can be A/D converted is 4 MHz. Thus the DAU could potentially provide data for a 4 MHz spectrum with a frequency resolution of approximately 2 KHz.

If the signal to be analyzed is a larger BW than that chosen by 1/d, then all signal components that lie outside the DFT BW will fold over and appear inside the DFT result. This is known as aliasing, a phenomenon that makes it critical that the signal being analyzed by filtered to the desired spectral bandwidth. For the SATCOM analyzer, the receiver, A25, has a maximum bandwidth of 1 MHz. If the entire satellite signal bandwidth were viewed with a sample rate of 1 MHz for a 2048 sample block the frequency resolution would be 500 Hz. To analyze a single channel of satellite signal a 10 KHz sample rate for a 256 sample block might typically be used. This would give a frequency resolution of 40 Hz over the 10 KHz bandwidth. If a 2048 block length were used for 10 KHz sample frequency, the frequency resolution is 5 Hz. Note that to filter the signal for a 10 KHz bandwidth requires a 5 KHz passband due to the dual channel operation. Also, if the signal is filtered at 5 KHz and sampled at 10 KHz, all signal components that appear in the filter skirts of the analog filter will appear aliased into the spectral output.

## C. THROUGHPUT

As indicated in the above discussion the accuracy of the DFT output involves a time/speed trade off. In order to produce a more accurate DFT output, the signal must be sampled longer (larger block size), which takes more time to sample and then a longer time to transfer and process that data before the next sample is started. Moreover, the processing time using the FFT algorithm increases proportionally to $N\log_2 N$.

Throughput is a measure of the amount of analyzed signal that can be sampled and processed relative to the amount of signal available. For example, if a signal is sampled in blocks of 1ØØ at a sample rate of 1Ø KHz; it takes approximately 1Ø milliseconds to collect the data. If it takes another 1Ø milliseconds to transfer the data, process the data and start a new sample block, then the system can be said to have a throughput of 5Ø percent. If thedata could be processed without missing a sample of data, the throughput would be 1ØØ percent or it would be a real time system.

The throughput of the SATCOM Signal Analyzer is a function not only on the DAU, but also the DMA transfer of data from the DAU to the INTERDATA, and then from the INTERDATA to the AP-12ØB, the AP processing time, the DMA transfer from the AP back to the INTERDATA, and finally the setup, transfer and plotting associated with the Graphics Display Terminal. An approximation for the throughput rate for this system, at a particular sample rate can be made by dividing the total known sample time by the total time necessary to achieve an output plot. As an example, for a block size of 256, the system throughput is approximately 1Ø% for the first bruteforce software. With software optimization it is expected that this will rise to approximately 50% for the current configuration. With the future direct DAU-AP interface, throughput for this case will be over 95%.

# V. FUTURE DESIGN MODIFICATIONS

## A. INTRODUCTION

The design goals for the SATCOM Signal Analyzer have been ordered in two major phases. The first phase called for an operational signal analyzer, including a working DAU integrated into the installed system devices. The first phase has been mostly completed as discussed by this report. The second phase is intended to optimize the system performance within the constraints of the present devices. The major thrust of phase two involves a modification of the DAU to allow acquired data to be stored directly into the AP-12ØB via the IOP-16 I/O port. With the DAU data sent directly to the AP-12ØB, a considerable amount of system overhead will be reduced, leaving the INTERDATA to perform control functions and greatly increasing the system throughput rates. The DAU modifications for phase two are mostly designed at the time of this writing with bench testing and circuit board construction scheduled to begin shortly /Ref. 15/.

## B. BASIC DAU MODIFICATIONS

### 1. IOP-16 Characteristics

The IOP-16, an I/O port included as an optional set of cards in the AP-12ØB chassis, provides for DMA data transfer to or from the AP under control of the AP or an external device. No dynamic interupt capability of the AP processor exists with the IOP-16 and the maximum DMA transfer rate is

1.5 million 16 bit words per second. The external address and data busses of the IOP-16 are compatible with the DEC PDP-11 Unibus structure.

2. DAU Modification Objectives

The present DAU is set up and controlled by the INTERDATA 7/32 via internal control registers. All addresses used on the DAU address bus are generated by the internal address bus and driven throughout the DAU. By using the IOP-16 interface as a smart device, under program control of the AP, the DAU control registers can be functionally loaded by the IOP-16. This effectively makes the IOP-16 the controller of the DAU via an AP program which is ultimately controlled from a user's program in the 7/32.

To minimize the lost processing time in the AP, a microcode AP program can start the DAU into an acquisition mode and continue to process data already stored in AP memory from a previous acquisition. Simultaneously the IOP, having started the DAU, will wait for an end of acquisition signal from the DAU, whereby the newly acquired data will automatically be DMA stored in the non-processing block of AP memory. After the AP has processed the current resident data, it will check to see if the new DMA is completed, and if so a new acquisition started if specified by the user FORTRAN program. During slow data rates, the IOP-16 will be capable of transferring out the new data directly after it is acquired on a word by word basis, making the new data available to the AP almost immediately after the A/D conversion. For the higher data rates, above 7ØØ KHz, the data will be transferred out by blocks after each block is acquired and stored in DAU buffer memory. The block transfers for high sample rates will not affect AP throughput because the processing time starts becoming longer than the acquisition time for those sample rates.

This modification to the DAU involves multiplexing of IOP-16 data and address lines into the DAU's present structure, plus additional control hardware. Utilization of the IOP-16 as a control interface for the DAU allows maximum AP processing effectiveness while requiring a minimum of hardware modification within the DAU.

## VI. CONCLUSION

The Data Acquisition Unit, subsystem of the SATCOM Signal Analyzer, has been completed to an operational state, and integrated into the SATCOM Signal Analyzer. Operational software has been provided to allow the system to be operated through a user interface with the computer terminal. This system, through high resolution, high speed, analog-to-digital conversion, using a dual channel conversion technique, has implemented digital spectrum analysis to significantly improve the capability of this laboratory for monitoring Navy satellite communications. All portions of this project have been passed on to incoming students in the laboratory for continuing design and construction.

# APPENDIX A

This appendix gives a complete pin to pin wiring list for the entire DAU. The DAU is comprises of 1Ø inch wide boards, numbered even, and 9 inch wide boards, numbered odd. Any given pin location in the DAU is designated by three numbers, i.e., 14-1-35 is pin 35 on connector 1 of board 14, a 1Ø inch board. The connectors and pins for each board are numbered as shown below. Auxiliary boards use the same pin numbering, but have only one connector, either connector 1 or 2. This appendix includes Table X, which is 37 pages.

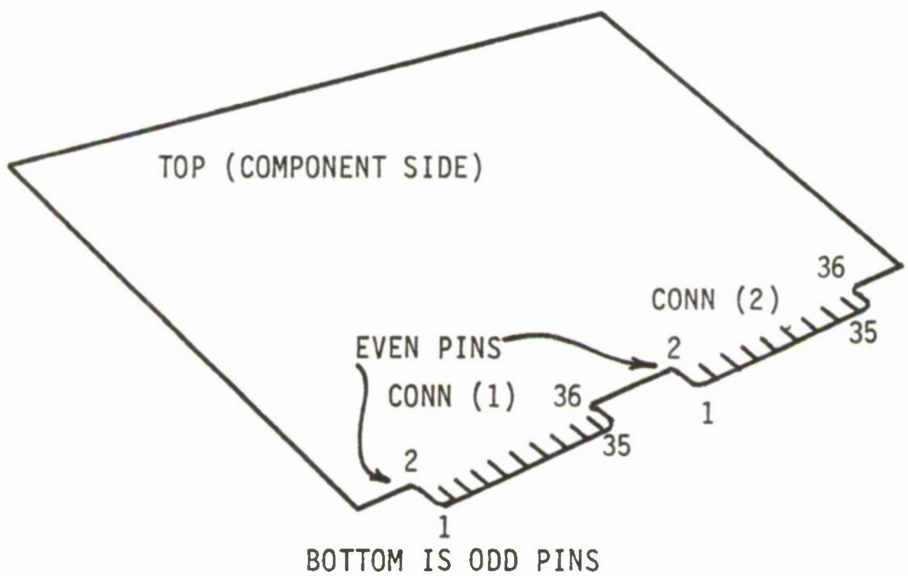


TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 1 of 38)

CONNECTOR (1)

| PIN | FUNCTION | TO | PIN | FUNCTION | TO |
|---|---|---|---|---|---|
| 12-1-2 | +5 | | 12-1-1 | Gnd | |
| 12-1-4 | +5 | | 12-1-3 | Gnd | |
| 12-1-6 | DRGØ | 16-1-15 | 12-1-5 | $\overline{\text{We}}$ In | 16-1-33 |
| 12-1-8 | Toggle FF IN (SEC) | 16-2-5 | 12-1-7 | $\overline{\text{We}}$ Out | 6-1-33 |
| 12-1-10 | DRG(Ø) B1 Out | 16-1-27 | 12-1-9 | $\overline{\text{We}}$ Out | 18-1-33 |
| 12-1-12 | DRG(Ø) B2 Out | 16-2-3 | 12-1-11 | NC | |
| 12-1-14 | $\overline{\text{CS}}$ | 6/18-2-2 | 12-1-13 | NC | |
| 12-1-16 | CS | 6/18-2-4 | 12-1-15 | Add In Bit 1 MSB | 10-1-17 |
| 12-1-18 | Add Out Bit 2 MSB | 6/18-1-31 | 12-1-17 | Add In Bit 2 MSB | 10-1-15 |
| 12-1-20 | Add Out Bit 3 | 6/18-1-29 | 12-1-19 | Add In Bit 3 | 10-1-13 |
| 12-1-22 | Add Out Bit 4 | 6/18-1-27 | 12-1-21 | Add In Bit 4 | 10-1-27 |
| 12-1-24 | Add Out Bit 5 | 6/18-1-25 | 12-1-23 | Add In Bit 5 | 10-1-25 |
| 12-1-26 | Add Out Bit 6 | 6/18-1-23 | 12-1-25 | Add In Bit 6 | 10-1-23 |
| 12-1-28 | Add Out Bit 7 | 6/18-1-21 | 12-1-27 | Add In Bit 7 | 10-1-21 |
| 12-1-30 | Add Out Bit 8 | 6/18-1-19 | 12-1-29 | Add In Bit 8 | 10-1-35 |
| 12-1-32 | Add Out Bit 9 | 6/18-1-17 | 12-1-31 | Add In Bit 9 | 10-1-33 |
| 12-1-34 | Add Out Bit 10 | 6/18-1-15 | 12-1-33 | Add In Bit 10 | 10-1-31 |
| 12-1-36 | Add Out Bit 11 LSB | 6/18-1-13 | 12-1-35 | Add In Bit 11 LSB | 10-1-29 |

AUXILIARY BOARD #1 DRIVERS

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 2 of 38)

CONNECTOR (2)

| PIN | FUNCTION | TO | PIN | FUNCTION | TO |
|---|---|---|---|---|---|
| 12-2-2 | NC | NC | 12-2-1 | NC | NC |
| 12-2-4 | NC | NC | 12-2-3 | NC | NC |
| 12-2-6 | NC | NC | 12-2-5 | NC | NC |
| 12-2-8 | NC | NC | 12-2-7 | NC | NC |
| 12-2-10 | NC | NC | 12-2-9 | NC | NC |
| 12-2-12 | NC | NC | 12-2-11 | NC | NC |
| 12-2-14 | NC | NC | 12-2-13 | NC | NC |
| 12-2-16 | NC | NC | 12-2-15 | NC | NC |
| 12-2-18 | NC | NC | 12-2-17 | NC | NC |
| 12-2-20 | NC | NC | 12-2-19 | NC | NC |
| 12-2-22 | NC | NC | 12-2-21 | NC | NC |
| 12-2-24 | NC | NC | 12-2-23 | NC | NC |
| 12-2-26 | SSYNCBØ In | 16-1-23 | 12-2-25 | NC | NC |
| 12-2-28 | SSYNCBØ(1) Out | 14-1-19<br>16-1-19 | 12-2-27 | SSYNCBØ(2) Out | 8-1-35 |
| 12-2-30 | ADC-Lo | 10-2-20 | 12-2-29 | $\overline{\text{BSEL}}$ Out | 4-1-12 |
| 12-2-32 | ADC-Hi | 10-2-16 | 12-2-31 | $\overline{\text{ASEL}}$ Out | 4-1-10 |
| 13-2-34 | +5 | | 12-2-33 | Gnd | Gnd |
| 12-2-36 | +5 | | 12-2-35 | Gnd | Gnd |

AUXILIARY BOARD #2 INVERTERS

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 3 of 38)

CONNECTOR (1)

| PIN | FUNCTION | TO | PIN | FUNC | TO |
|---|---|---|---|---|---|
| 2-1-2 | +5 | | 2-1-1 | Gnd | |
| 2-1-4 | +5 | | 2-1-3 | Gnd | |
| 2-1-6 | 1 MHz IN | 1-2-6 | 2-1-5 | NC | |
| 2-1-8 | SYNTEST In | 1-2-39 | 2-1-7 | NC | |
| 2-1-10 | NC | | 2-1-9 | NC | |
| 2-1-12 | SYNTEST 2 OUT | 9-1-35 | 2-1-11 | NC | |
| 2-1-14 | NC | | 2-1-13 | NC | |
| 2-1-16 | ADC2 LO | 10-2-22 | 2-1-15 | NC | |
| 2-1-18 | ADC2 HI | 10-2-28 | 2-1-17 | NC | |
| 2-1-20 | ADC3 LO | 16-2-23 | 2-1-19 | NC | |
| 2-1-22 | ADC3 HI | 16-2-19 | 2-1-21 | NC | |
| 2-1-24 | ADC HI | 10-2-16 | 2-1-23 | NC | |
| 2-1-26 | ADC LO | 10-2-20 | 2-1-25 | NC | |
| 2-1-28 | EOC HI CHN 2 | 16-2-11 | 2-1-27 | NC | |
| 2-1-30 | EOC LO CHN 1 | 16-2-27 | 2-1-29 | NC | |
| 2-1-32 | EOC LO CHN 2 | 10-2-25 | 2-1-31 | NC | |
| 2-1-34 | EOC HI CHN 1 | 10-2-13 | 2-1-33 | NC | |
| 2-1-36 | Gnd | | 2-1-35 | NC | |

ADC PRESTART CKT
AUXILIARY BOARD #3

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 4 of 38)

CONNECTOR (2)

| PIN | FUNCTION | | TO | PIN | FUNCTION | TO |
|---|---|---|---|---|---|---|
| 1-1-2 | +15 | P 18 | 11-2-36 | 1-1-1 | PWROK | 5-2-13 |
| 1-1-4 | RET | CH 1 | 11-2-35 | 1-1-3 | NC | 13-2-13 |
| 1-1-6 | -15 | | 11-2-34 | 1-1-5 | NC | 7-2-5 |
| 1-1-8 | +15 | P 19 | 5-2-36 | 1-1-7 | NC | 11-2-5 |
| 1-1-10 | RET | CH 2 | 5-2-35 | 1-1-9 | NC | Low Side Of |
| 1-1-12 | -15 | | 5-2-34 | 1-1-11 | NC | Front LED |
| 1-1-14 | +5 | P 20 | 11-2-10 | 1-1-13 | NC | |
| 1-1-16 | +5 RET | CH 1 | 11-2-9 | 1-1-15 | NC | |
| 1-1-18 | +5 | P 21 | 7-2-10 | 1-1-17 | NC | |
| 1-1-20 | +5 RET | CH 2 | 7-2-9 | 1-1-19 | NC | |
| 1-1-22 | -5 | P 17 | 7-2-14 | 1-1-21 | NC | |
| 1-1-24 | +5 RET | | 7-2-13 | 1-1-23 | NC | |
| 1-1-26 | +5 | Main Logic | 3-1-4 | 1-1-25 | NC | |
| 1-1-28 | +5 RET | P 16 | 3-1-3 | 1-1-27 | NC | |
| 1-1-30 | +10 | P 5 | 1-2-3 | 1-1-29 | NC | |
| 1-1-32 | +10 RET | | 1-2-12 | 1-1-31 | NC | |
| 1-1-34 | +24 | P 4 | 1-2-8 | 1-1-33 | NC | |
| 1-1-36 | +24 RET | | 1-2-12 | 1-1-35 | NC | |

ADC PROTECT CIRCUIT
AUXILIARY BOARD #4

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 5 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | SM101 PIN |
|---|---|---|---|
| 1-2-2 | Gnd | Gnd | Z |
| 1-2-4 | Gnd | Gnd | Y |
| 1-2-6 | 1 MHz In | J1, 2-1-6 | X |
| 1-2-8 | 24V In | +24V In, 1-1-33 | W |
| 1-2-10 | Gnd | Gnd | V |
| 1-2-12 | Gnd | Gnd, 1-1-31, 1-1-35 | U |
| 1-2-14 | Gnd | Gnd | T |
| 1-2-16 | 3rd MSD Bit 1 | 10-1-22 | S |
| 1-2-18 | Gnd | Gnd | R |
| 1-2-20 | Gnd | Gnd | P |
| 1-2-22 | Gnd | Gnd | N |
| 1-2-24 | 2nd MSD Bit 1 | 10-1-14 | M |
| 1-2-26 | Gnd | Gnd | L |
| 1-2-28 | Gnd | Gnd | K |
| 1-2-30 | Gnd | Gnd | J |
| 1-2-32 | Gnd | Gnd | H |
| 1-2-34 | Gnd | Gnd | F |
| 1-2-36 | Gnd | Gnd | E |
| 1-2-38 | Range Bit 1 | 10-1-11 | D |
| 1-2-40 | Range Bit 2 | 10-1-9 | C |
| 1-2-42 | Gnd | Gnd | B |
| 1-2-44 | Gnd | Gnd | A |

SYNTEST SM-101
DAU BOARD 1-2

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 6 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | SM101 PIN |
|---|---|---|---|
| 1-2-1 | Gnd | Gnd | 22 |
| 1-2-3 | +10 V In | +10 V, 1-1-29 | 21 |
| 1-2-5 | +5 V Out | NC | 20 |
| 1-2-7 | LSD Bit 2 | 10-1-32 | 19 |
| 1-2-9 | 3rd MSD Bit 2 | 10-1-24 | 18 |
| 1-2-11 | 3rd MSD Bit 4 | 10-1-26 | 17 |
| 1-2-13 | 3rd MSD Bit 8 | 10-1-28 | 16 |
| 1-2-15 | LSD Bit 8 | 10-1-36 | 15 |
| 1-2-17 | LSD Bit 4 | 10-1-34 | 14 |
| 1-2-19 | LSD Bit 1 | 10-1-30 | 13 |
| 1-2-21 | MSD Bit 2 | 10-1-8 | 12 |
| 1-2-23 | 2nd MSD Bit 2 | 10-1-16 | 11 |
| 1-2-25 | 2nd MSD Bit 8 | 10-1-20 | 10 |
| 1-2-27 | 2nd MSD Bit 4 | 10-1-18 | 9 |
| 1-2-29 | MSD Bit 8 | 10-1-12 | 8 |
| 1-2-31 | MSD Bit 4 | 10-1-10 | 7 |
| 1-2-33 | MSD Bit 1 | 10-1-6 | 6 |
| 1-2-35 | Range Bit 4 | 10-1-5 | 5 |
| 1-2-37 | Output Enable | NC | 4 |
| 1-2-39 | Output | 2-1-8 | 3 |
| 1-2-41 | Aux Output | NC | 2 |
| 1-2-43 | Gnd | Gnd | 1 |

SYNTEST SM-101
DAU BOARD 1-2

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 7 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 4-1-2 | Gnd | | 4-1-1 | +5 | |
| 4-1-4 | Gnd | | 4-1-3 | +5 | |
| 4-1-6 | NC | | 4-1-5 | NC | |
| 4-1-8 | NC | | 4-1-7 | NC | |
| 4-1-10 | A Sel | 12-2-31 | 4-1-9 | NC | |
| 4-1-12 | B Sel | 12-2-29 | 4-1-11 | NC | |
| 4-1-14 | Out Bit 0 MSB | 6-1-14 | 4-1-13 | Lo In Bit 1 | 5-1-8 |
| 4-1-16 | Out Bit 1 | 6-1-16 | 4-1-15 | Hi In Bit 1 | 7-1-8 |
| 4-1-18 | Out Bit 2 | 6-1-18 | 4-1-17 | Hi In Bit 0 MSB | 7-1-10 |
| 4-1-20 | Out Bit 3 | 6-1-20 | 4-1-19 | Lo In Bit 0 MSB | 5-1-10 |
| 4-1-22 | Out Bit 4 | 6-1-22 | 4-1-21 | Hi In Bit 2 | 7-1-14 |
| 4-1-24 | Out Bit 5 | 6-1-24 | 4-1-23 | Lo In Bit 2 | 5-1-14 |
| 4-1-26 | Out Bit 6 | 6-1-26 | 4-1-25 | Lo In Bit 3 | 5-1-12 |
| 4-1-28 | Out Bit 7 | 6-1-28 | 4-1-27 | Hi In Bit 3 | 7-1-12 |
| 4-1-30 | Out Bit 8 | 6-1-30 | 4-1-29 | Hi In Bit 5 | 7-1-16 |
| 4-1-32 | Out Bit 9 | 6-1-32 | 4-1-31 | Hi In Bit 4 | 7-1-18 |
| 4-1-34 | Out Bit 10 | 6-1-34 | 4-1-33 | Lo In Bit 4 | 5-1-18 |
| 4-1-36 | Out Bit 11 | 6-1-36 | 4-1-35 | Lo In Bit 5 | 5-1-16 |

BUFFER MEMORY INPUT CIRCUIT CHN 2
DAU BOARD #4

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 8 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 4-2-2 | 7/32 In Bit 0 MSB | B-2-48 | 4-2-1 | Lo In Bit 6 | 5-1-22 |
| 4-2-4 | 7/32 In Bit 1 | B-2-46 | 4-2-3 | Lo In Bit 7 | 5-1-20 |
| 4-2-6 | 7/32 In Bit 2 | B-2-44 | 4-2-5 | Hi In Bit 7 | 7-1-20 |
| 4-2-8 | 7/32 In Bit 3 | B-2-42 | 4-2-7 | Hi In Bit 6 | 7-1-22 |
| 4-2-10 | 7/32 In Bit 4 | B-2-40 | 4-2-9 | Hi In Bit 8 | Gnd |
| 4-2-12 | 7/32 In Bit 5 | B-2-38 | 4-2-11 | Lo In Bit 8 | 5-1-26 |
| 4-2-14 | 7/32 In Bit 6 | B-2-36 | 4-2-13 | Lo In Bit 9 | 5-1-24 |
| 4-2-16 | 7/32 In Bit 7 | B-2-34 | 4-2-15 | Hi In Bit 9 | Gnd |
| 4-2-18 | 7/32 In Bit 8 | B-2-17 | 4-2-17 | Lo In Bit 11 | 5-1-28 |
| 4-2-20 | 7/32 In Bit 9 | B-2-16 | 4-2-19 | Hi In Bit 11 | Gnd |
| 4-2-22 | 7/32 In Bit 10 | B-2-15 | 4-2-21 | Hi In Bit 10 | Gnd |
| 4-2-24 | 7/32 In Bit 11 | B-2-14 | 4-2-23 | Lo In Bit 11 | 5-1-30 |
| 4-2-26 | Clock In | 16-1-31 | 4-2-25 | NC | |
| 4-2-28 | NC | | 4-2-27 | NC | |
| 4-2-30 | NC | | 4-2-29 | NC | |
| 4-2-32 | NC | | 4-2-31 | NC | |
| 4-2-34 | Gnd | | 4-2-33 | +5 | |
| 4-2-36 | Gnd | | 4-2-35 | +5 | |

BUFFER MEMORY INPUT CIRCUIT CHN 2
DAU BOARD #4

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 9 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 5-1-2 | +5 to Logic | +5 | 5-1-1 | Gnd | Gnd |
| 5-1-4 | +5 to Logic | +5 | 5-1-3 | Gnd | Gnd |
| 5-1-6 | NC | NC | 5-1-5 | Gnd | Gnd |
| 5-1-8 | Out Bit 1 | 4-1-13 | 5-1-7 | Gnd | Gnd |
| 5-1-10 | Out Bit 0 MSB | 4-1-19 | 5-1-9 | Gnd | Gnd |
| 5-1-12 | Out Bit 3 | 4-1-25 | 5-1-11 | Gnd | Gnd |
| 5-1-14 | Out Bit 2 | 4-1-23 | 5-1-13 | Gnd | Gnd |
| 5-1-16 | Out Bit 5 | 4-1-35 | 5-1-15 | Gnd | Gnd |
| 5-1-18 | Out Bit 4 | 4-2-33 | 5-1-17 | Gnd | Gnd |
| 5-1-20 | Out Bit 7 | 4-2-3 | 5-1-19 | Gnd | Gnd |
| 5-1-22 | Out Bit 6 | 4-2-1 | 5-1-21 | Gnd | Gnd |
| 5-1-24 | Out Bit 9 | 4-2-13 | 5-1-23 | Gnd | Gnd |
| 5-1-26 | Out Bit 8 | 4-2-11 | 5-1-25 | Gnd | Gnd |
| 5-1-28 | Out Bit 11 LSB | 4-2-17 | 5-1-27 | Gnd | Gnd |
| 5-1-30 | Out Bit 10 | 4-2-23 | 5-1-29 | Gnd | Gnd |
| 5-1-32 | NC | NC | 5-1-31 | Gnd | Gnd |
| 5-1-34 | EOC | 16-2-25 | 5-1-33 | Gnd | Gnd |
| 5-1-36 | $\overline{\text{EOC}}$ | NC | 5-1-35 | Gnd | Gnd |

LOW SPEED ADC CIRCUIT CHN 2
DAU BOARD 5

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 10 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 5-2-2 | +5 to ADC | +5 to A/D | 5-2-1 | Gnd | Gnd |
| 5-2-4 | Start Conv | 9-1-15 | 5-2-3 | Start Conv Ret | 9-1-17 |
| 5-2-6 | Sample Comm | 9-1-27 | 5-2-5 | Gnd | 9-1-25 |
| 5-2-8 | NC | NC | 5-2-7 | NC | NC |
| 5-2-10 | NC | NC | 5-2-9 | +5 for Prot Rel | +5 |
| 5-2-12 | NC | NC | 5-2-11 | NC | NC |
| 5-2-14 | NC | NC | 5-2-13 | +5 Ret for Prot Rel | Gnd 1-1-1 |
| 5-2-16 | NC | NC | 5-2-15 | NC | NC |
| 5-2-18 | NC | NC | 5-2-17 | NC | NC |
| 5-2-20 | NC | NC | 5-2-19 | NC | NC |
| 5-2-22 | NC | NC | 5-2-21 | NC | NC |
| 5-2-24 | NC | NC | 5-2-23 | Gnd | NC |
| 5-2-26 | Analog In | 7-2-8, J9 | 5-2-25 | Gnd | 7-2-7 J9 Ret |
| 5-2-28 | NC | NC | 5-2-27 | NC | NC |
| 5-2-30 | NC | NC | 5-2-29 | NC | NC |
| 5-2-32 | NC | NC | 5-2-31 | NC | NC |
| 5-2-34 | -15 to S/H | 1-1-12 -15 to S/H | 5-2-23 | Gnd | Gnd |
| 5-2-36 | +15 to S/H | 1-1-8 +15 to S/H | 5-2-35 | Gnd | Gnd |

LOW SPEED ADC CIRCUIT CHN 2
DAU BOARD 5

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 11 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 6-1-2 | +5 | +5 | 6-1-1 | Gnd | Gnd |
| 6-1-4 | +5 | +5 | 6-1-3 | Gnd | Gnd |
| 6-1-6 | NC | NC | 6-1-5 | NC | NC |
| 6-1-8 | NC | NC | 6-1-7 | NC | NC |
| 6-1-10 | NC | NC | 6-1-9 | NC | NC |
| 6-1-12 | NC | NC | 6-1-11 | NC | NC |
| 6-1-14 | Data In Bit 0 | 4-1-14 | 6-1-13 | Add In Bit 11 LSB | 12-1-36 |
| 6-1-16 | Data In Bit 1 | 4-1-16 | 6-1-15 | Add In Bit 10 | 12-1-34 |
| 6-1-18 | Data In Bit 2 | 4-1-18 | 6-1-17 | Add In Bit 9 | 12-1-32 |
| 6-1-20 | Data In Bit 3 | 4-1-20 | 6-1-19 | Add In Bit 8 | 12-1-30 |
| 6-1-22 | Data In Bit 4 | 4-1-22 | 6-1-21 | Add In Bit 7 | 12-1-28 |
| 6-1-24 | Data In Bit 5 | 4-1-24 | 6-1-23 | Add In Bit 6 | 12-1-26 |
| 6-1-26 | Data In Bit 6 | 4-1-26 | 6-1-25 | Add In Bit 5 | 12-1-24 |
| 6-1-28 | Data In Bit 7 | 4-1-28 | 6-1-27 | Add In Bit 4 | 12-1-22 |
| 6-1-30 | Data In Bit 8 | 5-1-30 | 6-1-29 | Add In Bit 3 | 12-1-20 |
| 6-1-32 | Data In Bit 9 | 4-1-32 | 6-1-31 | Add In Bit 2 MSB | 12-1-18 |
| 6-1-34 | Data In Bit 10 | 4-1-34 | 6-1-33 | $\overline{WE}$ In | 12-1-7 |
| 6-1-36 | Data In Bit 11 | 4-1-36 | 6-1-35 | NC | NC |

BUFFER MEMORY CIRCUIT CHN 2
DAU BOARD #6

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 12 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 6-2-2 | $\overline{CS}$ In | 12-1-14 | 6-2-1 | NC | NC |
| 6-2-4 | CS In | 12-1-16 | 6-2-3 | NC | NC |
| 6-2-6 | Data Out Bit 0 MSB | 14-1-21 | 6-2-5 | NC | NC |
| 6-2-8 | Data Out Bit 1 | 14-1-23 | 6-2-7 | NC | NC |
| 6-2-10 | Data Out Bit 2 | 14-1-25 | 6-2-9 | NC | NC |
| 6-2-12 | Data Out Bit 3 | 14-1-27 | 6-2-11 | NC | NC |
| 6-2-14 | Data Out Bit 4 | 14-2-1 | 6-2-13 | NC | NC |
| 6-2-16 | Data Out Bit 5 | 14-2-3 | 6-2-15 | NC | NC |
| 6-2-18 | Data Out Bit 6 | 14-2-5 | 6-2-17 | NC | NC |
| 6-2-20 | Data Out Bit 7 | 14-2-7 | 6-2-19 | NC | NC |
| 6-2-22 | Data Out Bit 8 | 14-2-17 | 6-2-21 | NC | NC |
| 6-2-24 | Data Out Bit 9 | 14-2-19 | 6-2-23 | NC | NC |
| 6-2-26 | Data Out Bit 10 | 14-2-21 | 6-2-25 | NC | NC |
| 6-2-28 | Data Out Bit 11 | 14-2-23 | 6-2-27 | NC | NC |
| 6-2-30 | NC | NC | 6-2-29 | NC | NC |
| 6-2-32 | NC | NC | 6-2-31 | NC | NC |
| 6-2-34 | +5 | +5 | 6-2-33 | Gnd | Gnd |
| 6-2-36 | +5 | +5 | 6-2-35 | Gnd | Gnd |

BUFFER MEMORY CIRCUIT CHN 2
DAU BOARD #6

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 13 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 7-1-2 | +5 | +5 | 7-1-1 | Gnd | Gnd |
| 7-1-4 | +5 | +5 | 7-1-3 | Gnd | Gnd |
| 7-1-6 | $\overline{\text{EOC}}$ Out | NC | 7-1-5 | Gnd | Gnd |
| 7-1-8 | A/D Out Bit 1 | 4-1-15 | 7-1-7 | Gnd | Gnd |
| 7-1-10 | A/D Out Bit 0 MSB | 4-1-17 | 7-1-9 | Gnd | Gnd |
| 7-1-12 | A/D Out Bit 3 | 4-1-27 | 7-1-11 | Gnd | Gnd |
| 7-1-14 | A/D Out Bit 2 | 4-1-21 | 7-1-13 | Gnd | Gnd |
| 7-1-16 | A/D Out Bit 5 | 4-1-29 | 7-1-15 | Gnd | Gnd |
| 7-1-18 | A/D Out Bit 4 | 4-1-31 | 7-1-17 | Gnd | Gnd |
| 7-1-20 | A/D Out Bit 7 | 4-2-5 | 7-1-19 | Gnd | Gnd |
| 7-1-22 | A/D Out Bit 6 | 4-2-7 | 7-1-21 | Gnd | Gnd |
| 7-1-24 | NC | NC | 7-1-23 | Gnd | Gnd |
| 7-1-26 | NC | NC | 7-1-25 | Gnd | Gnd |
| 7-1-28 | NC | NC | 7-1-27 | GNd | Gnd |
| 7-1-30 | NC | NC | 7-1-29 | Gnd | Gnd |
| 7-1-32 | NC | NC | 7-1-31 | Gnd | Gnd |
| 7-1-34 | EOC Out | 16-2-11 | 7-1-33 | Gnd | Gnd |
| 7-1-36 | NC | NC | 7-1-35 | Gnd | Gnd |

HIGH SPEED ADC CIRCUIT CHN 2
DAU BOARD #7

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 14 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 7-2-2 | NC | NC | 7-2-1 | Gnd | Gnd |
| 7-2-4 | Start Conv | 9-2-29 | 7-2-3 | +5 to Protect Relay | Gnd |
| 7-2-6 | NC | NC | 7-2-5 | +5 Ret Prot Relay | Gnd |
| 7-2-8 | Rockland to HP 122Ø | 5-2-26 | 7-2-7 | Rockland Ret | Gnd 5-2-25 |
| 7-2-10 | +5 | +5 | 7-2-9 | Gnd Return +5 | Gnd |
| 7-2-12 | +5 | +5 | 7-2-11 | Gnd Return +5 | Gnd |
| 7-2-14 | -5 | -5 | 7-2-13 | Gnd Return -5 | Gnd |
| 7-2-16 | +15 | +15 | 7-2-15 | Gnd Return +15 | Gnd |
| 7-2-18 | -15 | -15 | 7-2-17 | Gnd Return -15 | Gnd |
| 7-2-20 | +5 | -15 | 7-2-19 | Gnd Return +5 | Gnd |
| 7-2-22 | To Ext in Switch | Front Panel | 7-2-21 | Ext in Switch Gnd Side | Gnd |
| 7-2-24 | Ext In Signal | Front Panel | 7-2-23 | Norm In Switch Gnd Side | Gnd |
| 7-2-26 | Analog to HP 122Ø | J-11 | 7-2-25 | HP 122Ø Ret | Gnd |
| 7-2-28 | Analog to Rockland | J-8 | 7-2-27 | Rockland Out Ret | Gnd |
| 7-2-30 | Norm Side Ext Switch | Front Panel | 7-2-29 | NC | Gnd |
| 7-2-32 | S/H Comm In | 9-2-9 | 7-2-31 | S/H Comm Ret | Gnd |
| 7-2-34 | -15 | -15 | 7-2-33 | Gnd Return -15 | Gnd |
| 7-2-36 | +15 | +15 | 7-2-35 | Gnd Return +15 | Gnd |

HIGH SPEED ADC CIRCUIT CHN 2
DAU BOARD #7

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 15 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 8-1-2 | +5 | +5 | 8-1-1 | Gnd | Gnd |
| 8-1-4 | +5 | +5 | 8-1-3 | Gnd | Gnd |
| 8-1-6 | NC | NC | 8-1-5 | DAGØ(5) B Out | 16-1-11 |
| 8-1-8 | NC | NC | 8-1-7 | COT Ø4Ø In | B-2-9 |
| 8-1-10 | NC | NC | 8-1-9 | COT Ø5Ø In | B-2-8 |
| 8-1-12 | NC | NC | 8-1-11 | COT Ø6Ø In | B-2-7 |
| 8-1-14 | NC | NC | 8-1-13 | COT Ø7Ø In | B-2-6 |
| 8-1-16 | NC | NC | 8-1-15 | DAG Ø In | B-2-5 |
| 8-1-18 | NC | NC | 8-1-17 | DAG Ø-(Ø) Out | 16-1-13 |
| 8-1-20 | NC | NC | 8-1-19 | DAG Ø-(1) Out | 10-2-12 |
| 8-1-22 | NC | NC | 8-1-21 | DAG Ø-(2) Out | 10-2-14 |
| 8-1-24 | NC | NC | 8-1-23 | DAG Ø-(3) Out | 10-2-10 |
| 8-1-26 | NC | NC | 8-1-25 | DAG Ø-(4) Out | 10-2-6 |
| 8-1-28 | NC | NC | 8-1-27 | DAG Ø-(5) Out | 10-2-24 |
| 9-1-30 | NC | NC | 8-1-29 | SIN Ø4Ø Out | B-3-5 |
| 8-1-32 | NC | NC | 8-1-31 | SATNO Out | B-2-3 |
| 8-1-34 | NC | NC | 8-1-33 | ØVØ SIN Ø5Ø Out | B-3-4 |
| 8-1-36 | NC | NC | 8-1-35 | SSYNØBØ In | 12-2-27 |

DATA ACQUISITION CONTROL CIRCUIT (1 of 2)
DAU BOARD #8

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 16 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 8-2-2 | NC | NC | 8-2-1 | EOC-LO CHN 2 In | 5-1-34 |
| 8-2-4 | NC | NC | 8-2-3 | EOC-LO CHN 1 In | 13-1-34 |
| 8-2-6 | NC | NC | 8-2-5 | EOC-HI CHN 2 In | 7-1-34 |
| 8-2-8 | NC | NC | 8-2-7 | EOC-LO CHN 1 In | 11-1-34 |
| 8-2-10 | NC | NC | 8-2-9 | WC-LO | NC |
| 8-2-12 | NC | NC | 8-2-11 | NC | NC |
| 8-2-14 | NC | NC | 8-2-13 | $\overline{E}$ Add Out | 10-2-2 |
| 8-2-16 | NC | NC | 8-2-15 | $\overline{E}$ WC Out | 10-2-8 |
| 8-2-18 | NC | NC | 8-2-17 | Busy In | 16-1-17 |
| 8-2-20 | NC | NC | 8-2-19 | EOM SIN Ø6Ø In | B-3-3 |
| 8-2-22 | NC | NC | 8-2-21 | WC M/M In | 10-2-18 |
| 8-2-24 | NC | NC | 8-2-23 | 7/32 WR In | 10-2-30 |
| 8-2-26 | NC | NC | 8-2-25 | 7/32 RD In | 10-2-26 |
| 8-2-28 | NC | NC | 8-2-27 | ADC2-LO-In | 10-2-20 |
| 8-2-30 | NC | NC | 8-2-29 | ADC2-HI-In | 10-2-16 |
| 8-2-32 | NC | NC | 8-2-31 | NC | NC |
| 8-2-34 | +5 | +5 | 8-2-33 | Gnd | Gnd |
| 8-2-36 | +5 | +5 | 8-2-35 | Gnd | Gnd |

DATA ACQUISITION CONTROL CIRCUIT (1 of 2)
DAU BOARD #8

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 17 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 9-1-2 | +5 | +5 | 9-1-1 | Gnd | Gnd |
| 9-1-4 | +5 | +5 | 9-1-3 | Gnd | Gnd |
| 9-1-6 | NC | NC | 9-1-5 | NC | NC |
| 9-1-8 | NC | NC | 9-1-7 | A/D LO CHN 1 Out | 13-2-4 |
| 9-1-10 | Gnd | Gnd | 9-1-9 | Gnd Ret From 9-1-7 | 13-2-3 |
| 9-1-12 | NC | NC | 9-1-11 | NC | NC |
| 9-1-14 | NC | NC | 9-1-13 | NC | NC |
| 9-1-16 | NC | NC | 9-1-15 | A/D LO CHN 2 Out | 5-2-4 |
| 9-1-18 | Gnd | Gnd | 9-1-17 | Gnd Ret From 9-1-15 | 5-2-3 |
| 9-1-20 | NC | NC | 9-1-19 | S/H LO CHN 1 Out | 13-2-6 |
| 9-1-22 | Gnd | Gnd | 9-1-21 | Gnd Ret for 9-1-19 | 13-2-5 |
| 9-1-24 | NC | NC | 9-1-23 | NC | NC |
| 9-1-26 | Gnd | Gnd | 9-1-25 | Gnd Ret for 9-1-27 | 5-2-5 |
| 9-1-28 | NC | NC | 9-1-27 | S/H LO CHN 2 Out | 5-2-6 |
| 9-1-30 | NC | NC | 9-1-29 | NC | NC |
| 9-1-32 | NC | NC | 9-1-31 | ADC2 LO In | 8-2-27 |
| 9-1-34 | NC | NC | 9-1-33 | ADC2 HI In | 8-2-29 |
| 9-1-36 | NC | NC | 9-1-35 | SYNTEST2 In | 1-1-39 |

ADC TIMING CIRCUIT
DAU BOARD #9

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 18 of 33)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 9-2-2 | NC | NC | 9-2-1 | NC | NC |
| 9-2-4 | NC | NC | 9-2-3 | S/H HI CHN 1 Out | 11-2-32 |
| 9-2-6 | Gnd | Gnd | 9-2-5 | Gnd Ret for 9-2-5 | 11-2-31 |
| 9-2-8 | Gnd | Gnd | 9-2-7 | Gnd Ret for 9-2-9 | 7-2-31 |
| 9-2-10 | NC | NC | 9-2-9 | S/H HI CHN 2 Out | 7-2-32 |
| 9-2-12 | NC | NC | 9-2-11 | NC | NC |
| 9-2-14 | NC | NC | 9-2-13 | NC | NC |
| 9-2-16 | NC | NC | 9-2-15 | NC | NC |
| 9-2-18 | NC | NC | 9-2-17 | NC | NC |
| 9-2-20 | Gnd | Gnd | 9-2-19 | Gnd Ret for 9-2-21 | 11-2-3 |
| 9-2-22 | NC | NC | 9-2-21 | ADC HI CHN 1 Out | 11-2-4 |
| 9-2-24 | NC | NC | 9-2-23 | NC | NC |
| 9-2-26 | NC | NC | 9-2-25 | NC | NC |
| 9-2-28 | Gnd | Gnd | 9-2-27 | Gnd Ret for 9-2-29 | 7-2-3 |
| 9-2-30 | NC | NC | 9-2-29 | ADC HI CHN 2 Out | 7-2-4 |
| 9-2-32 | NC | NC | 9-2-31 | NC | NC |
| 9-2-34 | +5 | +5 | 9-2-33 | Gnd | Gnd |
| 9-2-36 | +5 | +5 | 9-2-35 | Gnd | Gnd |

ADC TIMING CIRCUIT
DAU BOARD #9

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 19 of 38)

CONNECTOR (1)

| FROM | FUNCTION | | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|---|
| 10-1-2 | +5 | | +5 | 10-1-1 | Gnd | Gnd |
| 10-1-4 | +5 | | +5 | 10-1-3 | Gnd | Gnd |
| 10-1-6 | Freq Sel Bit 1 | | 1-2-33 | 10-1-5 | Range Out Bit 4 | 1-2-35 |
| 10-1-8 | Freq Sel Bit 2 | MSD | 1-2-21 | 10-1-7 | Range Out Bit 8 | NC |
| 10-1-10 | Freq Sel Bit 4 | OUT | 1-2-31 | 10-1-9 | Range Out Bit 2 | 1-2-40 |
| 10-1-12 | Freq Sel Bit 8 | | 1-2-29 | 10-1-11 | Range Out Bit 1 | 1-2-38 |
| 10-1-14 | Freq Sel Bit 1 | 2ND | 1-2-24 | 10-1-13 | Add Out Bit 3 | 12-1-19 |
| 10-1-16 | Freq Sel Bit 2 | MSD | 1-2-23 | 10-1-15 | Add Out Bit 2 | 12-1-17 |
| 10-1-18 | Freq Sel Bit 4 | OUT | 1-2-27 | 10-1-17 | Add Out Bit 1 | 12-1-15 |
| 10-1-20 | Freq Sel Bit 8 | | 1-2-25 | 10-1-19 | Add Out Bit 0 MSB | NC |
| 10-1-22 | Freq Sel Bit 1 | 3RD | 1-2-16 | 10-1-21 | Add Out Bit 7 | 12-1-27 |
| 10-1-24 | Freq Sel Bit 2 | MSD | 1-2-9 | 10-1-23 | Add Out Bit 6 | 12-1-25 |
| 10-1-26 | Freq Sel Bit 4 | OUT | 1-2-11 | 10-1-25 | Add Out Bit 5 | 12-1-23 |
| 10-1-28 | Freq Sel Bit 8 | | 1-2-13 | 10-1-27 | Add Out Bit 4 | 12-1-21 |
| 10-1-30 | Freq Sel Bit 1 | | 1-2-19 | 10-1-29 | Add Out Bit 11 LSB | 12-1-35 |
| 10-1-32 | Freq Sel Bit 2 | LSD | 1-2-7 | 10-1-31 | Add Out Bit 10 | 12-1-33 |
| 10-1-34 | Freq Sel Bit 4 | OUT | 1-2-3 | 10-1-33 | Add Out Bit 9 | 12-1-31 |
| 10-1-36 | Freq Sel Bit 8 | | 1-2-4 | 10-1-35 | Add Out Bit 8 | 12-1-29 |

DATA ACQUISITION CONTROL CIRCUIT (2 of 2)
DAU BOARD #10

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 20 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 10-2-2 | $\overline{E}$ Add In | 8-2-13 | 10-2-1 | 7/32 In DOT 12Ø | B-2-13 |
| 10-2-4 | SSYNCB In | 8-1-35 | 10-2-3 | 7/32 In DOT 13Ø | B-2-12 |
| 10-2-6 | DAGØ (4) In | 8-1-25 | 10-2-5 | 7/32 In DOT 14Ø | B-2-11 |
| 10-2-8 | $\overline{E}$ WC In | 8-2-15 | 10-2-7 | 7/32 In DOT 15Ø | B-2-10 |
| 10-2-10 | DAGØ (3) In | 8-1-23 | 10-2-9 | 7/32 In DOT Ø8Ø | B-2-17 |
| 10-2-12 | DAGØ (1) In | 8-1-19 | 10-2-11 | 7/32 In DOT Ø9Ø | B-2-16 |
| 10-2-14 | DAGØ (2) In | 8-1-21 | 10-2-13 | 7/32 In DOT 1ØØ | B-2-15 |
| 10-2-16 | ADC-HI Out | 2-1-24, 12-2-32<br>8-2-29 | 10-2-15 | 7/32 In DOT 11Ø | B-2-14 |
| 10-2-18 | M/M WC Out | 8-2-21 | 10-2-17 | 7/32 In DOT Ø4Ø | B-2-40 |
| 10-2-20 | ADC-LO Out | 12-2-30, 2-1-26<br>8-2-27 | 10-2-19 | 7/32 In DOT Ø5Ø | B-2-38 |
| 10-2-22 | ADC2-LO Out | 2-1-16 | 10-2-21 | 7/32 In DOT Ø6Ø | B-2-36 |
| 10-2-24 | DAGØ (5) In | 8-2-27 | 10-2-23 | 7/32 In DOT Ø7Ø | B-2-34 |
| 10-2-26 | 7/32 RD Out | 8-2-25, 16-1-35 | 10-2-25 | 7/32 In DOT ØØØ | B-2-48 |
| 10-2-28 | ADC2-Hi Out | 9-1-33, 2-1-18 | 10-2-27 | 7/32 In DOT Ø1Ø | B-2-46 |
| 10-2-30 | 7/32 WR Out | 8-2-23 | 10-2-29 | 7/32 In DOT Ø2Ø | B-2-44 |
| 10-2-32 | Spare DOT Ø8Ø | NC | 10-2-31 | 7/32 In DOT Ø3Ø | B-2-42 |
| 10-2-34 | +5 | +5 | 10-2-33 | Gnd | Gnd |
| 10-2-36 | +5 | +5 | 10-2-35 | Gnd | Gnd |

DATA ACQUISITION CONTROL CIRCUIT (2 of 2)

DAU BOARD #1Ø

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 21 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 11-1-2 | +5 | +5 | 11-1-1 | Gnd | Gnd |
| 11-1-4 | +5 | +5 | 11-1-3 | Gnd | Gnd |
| 11-1-6 | $\overline{\text{EOC}}$ Out | NC | 11-1-5 | Gnd | Gnd |
| 11-1-8 | A/D Out Bit 1 | 20-1-15 | 11-1-7 | Gnd | Gnd |
| 11-1-10 | A/D Out Bit 0 MSB | 20-1-17 | 11-1-9 | Gnd | Gnd |
| 11-1-12 | A/D Out Bit 3 | 20-1-27 | 11-1-11 | Gnd | Gnd |
| 11-1-14 | A/D Out Bit 2 | 20-1-21 | 11-1-13 | Gnd | Gnd |
| 11-1-16 | A/D Out Bit 5 | 20-1-29 | 11-1-15 | Gnd | Gnd |
| 11-1-18 | A/D Out Bit 4 | 20-1-31 | 11-1-17 | Gnd | Gnd |
| 11-1-20 | A/D Out Bit 7 | 20-2-5 | 11-1-19 | Gnd | Gnd |
| 11-1-22 | A/D Out Bit 6 | 20-2-7 | 11-1-21 | Gnd | Gnd |
| 11-1-24 | NC | NC | 11-1-23 | Gnd | Gnd |
| 11-1-26 | NC | NC | 11-1-25 | Gnd | Gnd |
| 11-1-28 | NC | NC | 11-1-27 | Gnd | Gnd |
| 11-1-30 | NC | NC | 11-1-29 | Gnd | Gnd |
| 11-1-32 | NC | NC | 11-1-31 | Gnd | Gnd |
| 11-1-34 | EOC Out | 16-2-13 | 11-1-33 | Gnd | Gnd |
| 11-1-36 | NC | NC | 11-1-35 | Gnd | Gnd |

HIGH SPEED ADC CIRCUIT CHANNEL 1
DAU BOARD #11

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 22 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 11-2-2 | NC | NC | 11-2-1 | Gnd | Gnd |
| 11-2-4 | Start Conv | 9-2-21 | 11-2-3 | +5 to Protect Relay | Gnd |
| 11-2-6 | NC | NC | 11-2-5 | +5 Ret Prot Relay | Gnd |
| 11-2-8 | Rockland to HP 122Ø | 13-2-26 | 11-2-7 | Rockland Ret | Gnd 13-2-25 |
| 11-2-10 | +5 | +5, 1-1-14 | 11-2-9 | Gnd Return +5 | Gnd |
| 11-2-12 | +5 | +5 | 11-2-11 | Gnd Return +5 | Gnd |
| 11-2-14 | -5 | -5 | 11-2-13 | Gnd Return -5 | Gnd |
| 11-2-16 | +15 | +15 | 11-2-15 | Gnd Return +15 | Gnd |
| 11-2-18 | -15 | -15 | 11-2-17 | Gnd Return -15 | Gnd |
| 11-2-20 | +5 | +5 | 11-2-19 | Gnd Return +5 | Gnd |
| 11-2-22 | To Ext In Switch | Front Panel | 11-2-21 | Ext In Switch Gnd Side | Gnd |
| 11-2-24 | Ext in Signal | Front Panel | 11-2-23 | Norm In Switch Gnd Side | Gnd |
| 11-2-26 | Analog to HP 122Ø | J-10 | 11-2-25 | HP 122Ø Ret | Gnd |
| 11-2-28 | Analog to Rockland | J-6 | 11-2-27 | Rockland Out Ret | Gnd |
| 11-2-30 | Norm Side Ext Switch | Front Panel | 11-2-29 | NC | Gnd |
| 11-2-32 | S/H Comm In | 9-2-3 | 11-2-31 | S/H Comm Ret | Gnd |
| 11-2-34 | -15 | -15, 1-1-6 | 11-2-33 | Gnd Return -15 | Gnd |
| 11-2-36 | +15 | +15, 1-1-2 | 11-2-35 | Gnd Return +15 | Gnd |

HIGH SPEED ADC CIRCUIT CHANNEL 1
ADC BOARD #11

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 23 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 13-1-2 | +5 to Logic | +5 | 13-1-1 | Gnd | Gnd |
| 13-1-4 | +5 to Logic | +5 | 13-1-3 | Gnd | Gnd |
| 13-1-6 | NC | NC | 13-1-5 | Gnd | Gnd |
| 13-1-8 | Out Bit 1 | 20-1-13 | 13-1-7 | Gnd | Gnd |
| 13-1-10 | Out Bit Ø MSB | 20-1-19 | 13-1-9 | Gnd | Gnd |
| 13-1-12 | Out Bit 3 | 20-1-25 | 13-1-11 | Gnd | Gnd |
| 13-1-14 | Out Bit 2 | 20-1-23 | 13-1-13 | Gnd | Gnd |
| 13-1-16 | Out Bit 5 | 20-1-35 | 13-1-15 | Gnd | Gnd |
| 13-1-18 | Out Bit 4 | 20-1-33 | 13-1-17 | Gnd | Gnd |
| 13-1-20 | Out Bit 7 | 20-2-3 | 13-1-19 | Gnd | Gnd |
| 13-1-22 | Out Bit 6 | 20-2-1 | 13-1-21 | Gnd | Gnd |
| 13-1-24 | Out Bit 9 | 20-2-13 | 13-1-23 | Gnd | Gnd |
| 13-1-26 | Out Bit 8 | 20-2-11 | 13-1-25 | Gnd | Gnd |
| 13-1-28 | Out Bit 11 LSB | 20-2-17 | 13-1-27 | Gnd | Gnd |
| 13-1-30 | Out Bit 1Ø | 20-2-23 | 13-1-29 | Gnd | Gnd |
| 13-1-32 | NC | NC | 13-1-31 | Gnd | Gnd |
| 13-1-34 | EOC | 16-2-27 | 13-1-33 | Gnd | Gnd |
| 13-1-36 | $\overline{\text{EOC}}$ | NC | 13-1-35 | Gnd | Gnd |

LOW SPEED ADC CIRCUIT CHANNEL 1
DAU BOARD #13

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 24 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 13-2-2 | +5 to ADC | +5 to ADC | 13-2-1 | Gnd | Gnd |
| 13-2-4 | Start Conv | 9-1-7 | 13-2-3 | Sample Comm | 9-1-9 |
| 13-2-6 | Sample Comm | 9-1-19 | 13-2-5 | Gnd | 9-1-21 |
| | NC | NC | 13-2-7 | NC | NC |
| 13-2-10 | NC | NC | 13-2-9 | NC | +5 |
| 13-2-12 | NC | NC | 13-2-11 | NC | NC |
| 13-2-14 | NC | NC | 13-2-13 | NC | 1-1-1 |
| 13-2-16 | NC | NC | 13-2-15 | NC | NC |
| 13-2-18 | NC | NC | 13-2-17 | NC | NC |
| 13-2-20 | NC | NC | 13-2-19 | NC | NC |
| 13-2-22 | NC | NC | 13-2-21 | NC | NC |
| 13-2-24 | NC | NC | 13-2-23 | Gnd | NC |
| 13-2-26 | Analog In | 13-2-8, J7 | 13-2-25 | Gnd | 13-2-7 J7 Ret |
| 13-2-28 | NC | NC | 13-2-27 | NC | NC |
| 13-2-30 | NC | NC | 13-2-29 | NC | NC |
| 13-2-32 | NC | NC | 13-2-31 | NC | NC |
| 13-2-34 | -15 to S/H | -15 to S/H | 13-2-33 | Gnd | NC |
| 13-2-36 | +15 to S/H | +15 to S/H | 13-2-35 | Gnd | Gnd |

LOW SPEED ADC CIRCUIT CHANNEL 1
DAU BOARD #13

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 25 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 14-1-2 | +5 | +5 | 14-1-1 | Gnd | Gnd |
| 14-1-4 | +5 | +5 | 14-1-3 | Gnd | Gnd |
| 14-1-6 | NC | NC | 14-1-5 | NC | NC |
| 14-1-8 | NC | NC | 14-1-7 | NC | NC |
| 14-1-10 | NC | NC | 14-1-9 | NC | NC |
| 14-1-12 | NC | NC | 14-1-11 | NC | NC |
| 14-1-14 | AP Out Bit 4 | NC | 14-1-13 | NC | NC |
| 14-1-16 | AP Out Bit 5 | NC | 14-1-15 | AP Out Enable | Gnd |
| 14-1-18 | 7/32 Out Bit 4 | B-3-40 | 14-1-17 | Select In | 16-2-5 |
| 14-1-20 | 7/32 Out Bit 5 | B-3-38 | 14-1-19 | SSYNCBØ | 12-2-28 |
| 14-1-22 | 7/32 Out Bit 4 | B-3-42 | 14-1-21 | Chn 2 In Bit Ø MSB | 6-2-6 |
| 14-1-24 | 7/32 Out Bit Ø | B-2-1 | 14-1-23 | Chn 2 In Bit 1 | 6-2-8 |
| 14-1-26 | 7/32 Out Bit 1 | B-3-46 | 14-1-25 | Chn 2 In Bit 2 | 6-2-10 |
| 14-1-28 | 7/32 Out Bit 2 | B-3-44 | 14-1-27 | Chn 2 In Bit 3 | 6-2-12 |
| 14-1-30 | AP Out Bit 3 | NC | 14-1-29 | Chn 1 In Bit Ø MSB | 18-2-6 |
| 14-1-32 | AP Out Bit 2 | NC | 14-1-31 | Chn 1 In Bit 1 | 18-2-8 |
| 14-1-34 | AP Out Bit Ø | NC | 14-1-33 | Chn 1 In Bit 2 | 18-2-10 |
| 14-1-36 | AP Out Bit 1 | NC | 14-1-35 | Chn 1 In Bit 3 | 18-2-12 |

BUFFER MEMORY OUTPUT SELECTOR CIRCUIT
DAU BOARD #14

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 26 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 14-2-2 | AP Out Bit 11 | NC | 14-2-1 | Chn 2 In Bit 4 | 6-2-14 |
| 14-2-4 | AP Out Bit 1Ø | NC | 14-2-3 | Chn 2 In Bit 5 | 6-2-16 |
| 14-2-6 | AP Out Bit 8 | NC | 14-2-5 | Chn 2 In Bit 6 | 6-2-18 |
| 14-2-8 | AP Out Bit 9 | NC | 14-2-7 | Chn 2 In Bit 7 | 6-2-20 |
| 14-2-10 | 7/32 Out Bit 11 | B-3-14 | 14-2-9 | Chn 1 In Bit 4 | 18-2-14 |
| 14-2-12 | 7/32 Out Bit 1Ø | B-3-15 | 14-2-11 | Chn 1 In Bit 5 | 18-2-16 |
| 14-2-14 | 7/32 Out Bit 8 | B-3-17 | 14-2-13 | Chn 1 In Bit 6 | 18-2-18 |
| 14-2-16 | 7/32 Out Bit 9 | B-3-16 | 14-2-15 | Chn 1 In Bit 7 | 18-2-20 |
| 14-2-18 | 7/32 Out Bit 6 | B-3-36 | 14-2-17 | Chn 2 In Bit 8 | 6-2-22 |
| 14-2-20 | 7/32 Out Bit 7 | B-3-34 | 14-2-19 | Chn 2 In Bit 9 | 6-2-24 |
| 14-2-22 | AP Out Bit 7 | NC | 14-2-21 | Chn 2 In Bit 1Ø | 6-2-26 |
| 14-2-24 | AP Out Bit 6 | NC | 14-2-23 | Chn 2 In Bit 11 | 6-2-28 |
| 14-2-26 | NC | NC | 14-2-25 | Chn 1 In Bit 8 | 18-2-22 |
| 14-2-28 | NC | NC | 14-2-27 | Chn 1 In Bit 9 | 18-2-24 |
| 14-2-30 | NC | NC | 14-2-29 | Chn 1 In Bit 1Ø | 18-2-26 |
| 14-2-32 | NC | NC | 14-2-31 | Chn 1 In Bit 11 | 18-2-28 |
| 14-2-34 | +5 | +5 | 14-2-33 | Gnd | Gnd |
| 14-2-36 | +5 | +5 | 14-2-35 | Gnd | Gnd |

BUFFER MEMORY OUTPUT SELECTOR CIRCUIT
DAU BOARD #14

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 27 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 16-1-2 | +5 | +5 | 16-1-1 | Gnd | Gnd |
| 16-1-4 | +5 | +5 | 16-1-3 | Gnd | Gnd |
| 16-1-6 | NC | NC | 16-1-5 | Al In | 10-1-17 |
| 16-1-8 | NC | NC | 16-1-7 | NC | NC |
| 16-1-10 | NC | NC | 16-1-9 | NC | NC |
| 16-1-12 | NC | NC | 16-1-11 | DAG Ø (5) B In | 8-1-5 |
| 16-1-14 | NC | NC | 16-1-13 | DAG Ø (Ø) In | 8-1-17 |
| 16-1-16 | NC | NC | 16-1-15 | DRG Ø (Ø) In | 12-1-6, B-2-4 |
| 16-1-18 | NC | NC | 16-1-17 | Busy 1 Out | 8-2-17 |
| 16-1-20 | NC | NC | 16-1-19 | SSYNCBØ In | 12-2-28 |
| 16-1-22 | NC | NC | 16-1-21 | NC | NC |
| 16-1-24 | NC | NC | 16-1-23 | SSYNC BØ Out | 12-2-26 |
| 16-1-26 | NC | NC | 16-1-25 | SSYNC Al Out | NC |
| 16-1-28 | NC | NC | 16-1-27 | DRG (Ø) Bl In | 12-1-10 |
| 16-1-30 | NC | NC | 16-1-29 | DAG (Ø) Bl Out | 20-2-26 |
| 16-1-32 | NC | NC | 16-1-31 | DAG (Ø) B2 Out | 4-2-26 |
| 16-1-34 | NC | NC | 16-1-33 | $\overline{\text{WE}}$ Out | 12-1-5 |
| 16-1-36 | NC | NC | 16-1-35 | 7/32 RD In | 10-2-26 |

BUFFER MEMORY TIMING CIRCUIT
DAU BOARD #16

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 28 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 16-2-2 | NC | NC | 16-2-1 | NC | NC |
| 16-2-4 | NC | NC | 16-2-3 | DRG (Ø) B2 In | 12-1-12 |
| 16-2-6 | NC | NC | 16-2-5 | Sel Out | 12-1-8, 14-1-17 |
| 16-2-8 | NC | NC | 16-2-7 | NC | NC |
| 16-2-10 | NC | NC | 16-2-9 | NC | NC |
| 16-2-12 | NC | NC | 16-2-11 | EOC Hi Chn 2 In | 7-1-34, 2-1-28 |
| 16-2-14 | NC | NC | 16-2-13 | EOC Hi Chn 1 In | 11-1-34, 2-1-34 |
| 16-2-16 | NC | NC | 16-2-15 | NC | NC |
| 16-2-18 | NC | NC | 16-2-17 | ADC3 Hi In | NC |
| 16-2-20 | NC | NC | 16-2-19 | ADC3 Hi In | 2-1-22 |
| 16-2-22 | NC | NC | 16-2-21 | ADC3 Lo In | NC |
| 16-2-24 | NC | NC | 16-2-23 | ADC3 Lo In | 2-1-20 |
| 16-2-26 | NC | NC | 16-2-25 | EOC Lo Chn 2 In | 5-1-34, 2-1-32 |
| 16-2-28 | NC | NC | 16-2-27 | EOC Lo Chn 1 In | 13-1-34, 2-1-30 |
| 16-2-30 | NC | NC | 16-2-29 | NC | NC |
| 16-2-32 | NC | NC | 16-2-31 | NC | NC |
| 16-2-34 | +5 | +5 | 16-2-33 | Gnd | Gnd |
| 16-2-36 | +5 | +5 | 16-2-35 | Gnd | Gnd |

BUFFER MEMORY TIMING CIRCUIT
DAU BOARD #16

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 29 of 38)

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 18-1-2 | +5 | +5 | 18-1-1 | Gnd | Gnd |
| 18-1-4 | +5 | +5 | 18-1-3 | Gnd | Gnd |
| 18-1-6 | NC | NC | 18-1-5 | NC | NC |
| 18-1-8 | NC | NC | 18-1-7 | NC | NC |
| 18-1-10 | NC | NC | 18-1-9 | NC | NC |
| 18-1-12 | NC | NC | 18-1-11 | NC | NC |
| 18-1-14 | Data In Bit 0 MSB | 20-1-14 | 18-1-13 | Add In Bit 11 LSB | 12-1-36 |
| 18-1-16 | Data In Bit 1 | 20-1-16 | 18-1-15 | Add In Bit 10 | 12-1-34 |
| 18-1-18 | Data In Bit 2 | 20-1-18 | 18-1-17 | Add In Bit 9 | 12-1-32 |
| 18-1-20 | Data In Bit 3 | 20-1-20 | 18-1-19 | Add In Bit 8 | 12-1-30 |
| 18-1-22 | Data In Bit 4 | 20-1-22 | 18-1-21 | Add In Bit 7 | 12-1-28 |
| 18-1-24 | Data In Bit 5 | 20-1-24 | 18-1-23 | Add In Bit 6 | 12-1-26 |
| 18-1-26 | Data In Bit 6 | 20-1-26 | 18-1-25 | Add In Bit 5 | 12-1-24 |
| 18-1-28 | Data In Bit 7 | 20-1-28 | 18-1-27 | Add In Bit 4 | 12-1-22 |
| 18-1-30 | Data In Bit 8 | 20-1-30 | 18-1-29 | Add In Bit 3 | 12-1-20 |
| 18-1-32 | Data In Bit 9 | 20-1-32 | 18-1-31 | Add In Bit 2 MSB | 12-1-18 |
| 18-1-34 | Data In Bit 10 | 20-1-34 | 18-1-33 | $\overline{\text{We}}$ In | 12-1-9 |
| 18-1-36 | Data In Bit 11 | 20-1-36 | 18-1-35 | NC | NC |

BUFFER MEMORY CIRCUIT CHANNEL 1
DAU BOARD #18

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 30 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 18-2-2 | $\overline{CS}$ In | 12-1-14 | 18-2-1 | NC | NC |
| 18-2-4 | CS In | 12-1-16 | 18-2-3 | NC | NC |
| 18-2-6 | Data Out Bit 0 MSB | 14-1-29 | 18-2-5 | NC | NC |
| 18-2-8 | Data Out Bit 1 | 14-1-31 | 18-2-7 | NC | NC |
| 18-2-10 | Data Out Bit 2 | 14-1-33 | 18-2-9 | NC | NC |
| 18-2-12 | Data Out Bit 3 | 14-1-35 | 18-2-11 | NC | NC |
| 18-2-14 | Data Out Bit 4 | 14-2-9 | 18-2-13 | NC | NC |
| 18-2-16 | Data Out Bit 5 | 14-2-11 | 18-2-15 | NC | NC |
| 18-2-18 | Data Out Bit 6 | 14-2-13 | 18-2-17 | NC | NC |
| 18-2-20 | Data Out Bit 7 | 14-2-15 | 18-2-19 | NC | NC |
| 18-2-22 | Data Out Bit 8 | 14-2-25 | 18-2-21 | NC | NC |
| 18-2-24 | Data Out Bit 9 | 14-2-27 | 18-2-23 | NC | NC |
| 18-2-26 | Data Out Bit 1Ø | 14-2-29 | 18-2-25 | NC | NC |
| 18-2-28 | Data Out Bit 11 | 14-2-31 | 18-2-27 | NC | NC |
| 18-2-30 | NC | NC | 18-2-29 | NC | NC |
| 18-2-32 | NC | NC | 18-2-31 | NC | NC |
| 18-2-34 | +5 | +5 | 18-2-33 | Gnd | Gnd |
| 18-2-36 | +5 | +5 | 18-2-35 | Gnd | Gnd |

BUFFER MEMORY CIRCUIT
DAU BOARD #18

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 31 of 3 )

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 20-1-2 | Gnd | Gnd | 20-1-1 | +5 | +5 |
| 20-1-4 | Gnd | Gnd | 20-1-3 | +5 | +5 |
| 20-1-6 | NC | NC | 20-1-5 | NC | NC |
| 20-1-8 | NC | NC | 20-1-7 | NC | NC |
| 20-1-10 | A Sel | 12-2-31 | 20-1-9 | NC | NC |
| 20-1-12 | B Sel | 12-2-29 | 20-1-11 | NC | NC |
| 20-1-14 | Out Bit 0 MSB | 18-1-14 | 20-1-13 | Lo In Bit 1 | 13-1-8 |
| 20-1-16 | Out Bit 1 | 18-1-16 | 20-1-15 | Hi In Bit 1 | 11-1-8 |
| 20-1-18 | Out Bit 2 | 18-1-18 | 20-1-17 | Hi In Bit 0 MSB | 11-1-10 |
| 20-1-20 | Out Bit 3 | 18-1-29 | 20-1-19 | Lo In Bit 0 MSB | 13-1-10 |
| 20-1-22 | Out Bit 4 | 18-1-22 | 20-1-21 | Hi In Bit 2 | 11-1-14 |
| 20-1-24 | Out Bit 5 | 18-1-24 | 20-1-23 | Lo In Bit 2 | 13-1-14 |
| 20-1-26 | Out Bit 6 | 18-1-26 | 20-1-25 | Lo In Bit 3 | 13-1-12 |
| 20-1-28 | Out Bit 7 | 18-1-28 | 20-1-27 | Hi In Bit 3 | 11-1-12 |
| 20-1-30 | Out Bit 8 | 18-1-30 | 20-1-29 | Hi In Bit 5 | 11-1-16 |
| 20-1-32 | Out Bit 9 | 18-1-32 | 20-1-31 | Hi In Bit 4 | 11-1-18 |
| 20-1-34 | Out Bit 10 | 18-1-34 | 20-1-33 | Lo In Bit 4 | 13-1-18 |
| 20-1-36 | Out Bit 11 | 18-1-36 | 20-1-35 | Lo In Bit 5 | 13-1-16 |

BUFFER MEMORY INPUT SELECTOR CIRCUIT CHANNEL 1
DAU BOARD #20

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 32 of 38)

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 20-2-2 | 7/32 In Bit 0 MSB | B-2-48 | 20-2-1 | Lo In Bit 6 | 13-1-22 |
| 20-2-4 | 7/32 In Bit 1 | B-2-46 | 20-2-3 | Lo In Bit 7 | 13-1-20 |
| 20-2-6 | 7/32 In Bit 2 | B-2-44 | 20-2-5 | Hi In Bit 7 | 11-1-20 |
| 20-2-8 | 7/32 In Bit 3 | B-2-42 | 20-2-7 | Hi In Bit 6 | 11-1-22 |
| 20-2-10 | 7/32 In Bit 4 | B-2-40 | 20-2-9 | Hi In Bit 8 | Gnd (Hi Bit 9) |
| 20-2-12 | 7/32 In Bit 5 | B-2-38 | 20-2-11 | Lo In Bit 8 | 13-1-26 |
| 20-2-14 | 7/32 In Bit 6 | B-2-36 | 20-2-13 | Lo In Bit 9 | 13-1-24 |
| 20-2-16 | 7/32 In Bit 7 | B-2-34 | 20-2-15 | Hi In Bit 9 | Gnd (Hi Bit 1Ø) |
| 20-2-18 | 7/32 In Bit 8 | B-2-17 | 20-2-17 | Lo In Bit 11 | 13-1-28 |
| 20-2-20 | 7/32 In Bit 9 | B-2-16 | 20-2-19 | Hi In Bit 11 | Gnd (Hi Bit 12) |
| 20-2-22 | 7/32 In Bit 1Ø | B-2-15 | 20-2-21 | Hi In Bit 10 | Gnd (Hi Bit 11) |
| 20-2-24 | 7/32 In Bit 11 | B-2-14 | 20-2-23 | Lo In Bit 10 | 13-1-30 |
| 20-2-26 | Clock In | 16-1-29 | 20-2-25 | NC | NC |
| 20-2-28 | NC | NC | 20-2-27 | NC | NC |
| 20-2-30 | NC | NC | 20-2-29 | NC | NC |
| 20-2-32 | NC | NC | 20-2-31 | NC | NC |
| 20-2-34 | Gnd | Gnd | 20-2-33 | +5 | +5 |
| 20-2-36 | Gnd | Gnd | 20-2-35 | +5 | +5 |

BUFFER MEMORY INPUT SELECTOR CIRCUIT CHANNEL 1
DAU BOARD #20

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 33 of 38)

CONNECTOR (2) DD - 50S

| FUNC | FROM | TO | FUNC | FROM | TO |
|---|---|---|---|---|---|
| DIN ØØØ | B-2-1 | 14-1-24 | DIN ØØØ RET | B-2-18 | Gnd |
| SCLR Ø | B-2-2 | NC | SCLR Ø RET | B-2-19 | Gnd |
| SATNO Ø | B-2-3 | 8-1-31 | SATNO Ø RET | B-2-20 | Gnd |
| DRG Ø | B-2-4 | 16-1-15 | DRG Ø RET | B-2-21 | Gnd |
| DAG Ø | B-2-5 | 8-1-15 | DAG Ø RET | B-2-22 | 8-1-1, Gnd |
| COT Ø7Ø | B-2-6 | 8-1-13 | COT Ø7Ø RET | B-2-23 | Gnd |
| COT Ø6Ø | B-2-7 | 8-1-11 | COT Ø6Ø RET | B-2-24 | Gnd |
| COT Ø5Ø | B-2-8 | 8-1-9 | COT Ø5Ø RET | B-2-25 | Gnd |
| COT Ø4Ø | B-2-9 | 8-1-7 | COT Ø4Ø RET | B-2-26 | Gnd |
| DOT 15Ø | B-2-10 | 10-2-7 | DOT 15Ø RET | B-2-27 | Gnd |
| DOT 14Ø | B-2-11 | 10-2-5 | DOT 14Ø RET | B-2-28 | Gnd |
| DOT 13Ø | B-2-12 | 10-2-3 | DOT 13Ø RET | B-2-29 | Gnd |
| DOT 12Ø | B-2-13 | 10-2-1 | DOT 12Ø RET | B-2-30 | Gnd |

DAU BACKPLANE CONNECTOR PIN MAP (BACK-CONN - PIN)
INTERCONNECTION TO INTERDATA 7/32 ULI

TABLE XI - DAU PIN TO PIN WIRING TEST (Sheet 34 of 38)

CONNECTOR (2) DD - 50S

| FUNC | FROM | TO | FUNC | FROM | TO |
|---|---|---|---|---|---|
| DOT 11Ø | B-2-14 | 10-2-15<br>4/20-2-24 | DOT 11Ø RET | B-2-31 | Gnd |
| DOT 1ØØ | B-2-15 | 10-2-13<br>4/20-2-22 | DOT 1ØØ RET | B-2-32 | Gnd |
| DOT Ø9Ø | B-2-16 | 10-2-11<br>4/20-2-20 | DOT Ø9Ø RET | B-2-33 | Gnd |
| DOT Ø8Ø | B-2-17 | 10-2-9<br>4/20-2-18 | DOT Ø8Ø RET | B-2-50 | Gnd |
| DOT Ø7Ø | B-2-34 | 10-2-23<br>4/20-2-16 | DOT Ø7Ø RET | B-2-35 | Gnd |
| DOT Ø6Ø | B-2-36 | 10-2-21<br>4/20-2-14 | DOT Ø6Ø RET | B-2-37 | Gnd |
| DOT Ø5Ø | B-2-38 | 10-2-19<br>4/20-2-12 | DOT Ø5Ø RET | B-2-39 | Gnd |
| DOT Ø4Ø | B-2-40 | 10-2-17<br>4/20-2-10 | DOT Ø4Ø RET | B-2-41 | Gnd |
| DOT Ø3Ø | B-2-42 | 10-2-31<br>4/20-2-8 | DOT Ø3Ø RET | B-2-43 | Gnd |
| DOT Ø2Ø | B-2-44 | 10-2-29<br>4-20-2-6 | DOT Ø2Ø RET | B-2-45 | Gnd |
| DOT Ø1Ø | B-2-46 | 10-2-27<br>4/20-2-4 | DOT Ø1Ø RET | B-2-47 | Gnd |
| DOT ØØØ | B-2-48 | 10-2-25<br>4/20-2-2 | DOT ØØØ RET | B-2-49 | Gnd |

DAU BACKPLANE CONNECTOR PIN MAP (BACK-CONN - PIN)
INTERCONNECTION TO INTERDATA 7/32 ULI

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 35 of 38)

CONNECTOR (3) DD - 50S

| FUNC | FROM | TO | FUNC | FROM | TO |
|---|---|---|---|---|---|
| Gnd | B-3-1 | Gnd | Gnd | B-3-18 | Gnd |
| SIN Ø7Ø | B-3-2 | NC | SIN Ø7Ø RET | B-3-19 | Gnd |
| SIN Ø6Ø | B-3-3 | 8-2-19 | SIN Ø6Ø RET | B-3-20 | Gnd |
| SIN Ø5Ø | B-3-4 | 8-1-33 | SIN Ø5Ø RET | B-3-21 | Gnd |
| SIN Ø4Ø | B-3-5 | 8-1-29 | SIN Ø4Ø RET | B-3-22 | Gnd |
| SIN Ø3Ø | B-3-6 | NC | SIN Ø3Ø RET | B-3-23 | Gnd |
| SIN Ø2Ø | B-3-7 | NC | SIN Ø2Ø RET | B-3-24 | Gnd |
| SIN Ø1Ø | B-3-8 | NC | SIN Ø1Ø RET | B-3-25 | Gnd |
| SIN ØØØ | B-3-9 | NC | SIN ØØØ RET | B-3-26 | Gnd |
| SIN 15Ø | B-3-10 | Gnd | SIN 15Ø RET | B-3-27 | Gnd |
| SIN 14Ø | B-3-11 | Gnd | SIN 14Ø RET | B-3-28 | Gnd |
| SIN 13Ø | B-3-12 | Gnd | SIN 13Ø RET | B-3-29 | Gnd |

DAU BACKPLANE CONNECTOR PIN MAP (BACK-CONN - PIN)
INTERCONNECTION TO INTERDATA 7/32 ULI

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 36 of 38)

CONNECTOR (3) DD - 50S

| FUNC | FROM | TO | FUNC | FROM | TO |
|---|---|---|---|---|---|
| DIN 12Ø | B-3-13 | Gnd | DIN 12Ø RET | B-3-30 | Gnd |
| DIN 11Ø | B-3-14 | 14-2-10 | DIN 11Ø RET | B-3-31 | Gnd |
| DIN 1ØØ | B-3-15 | 14-2-12 | DIN 1ØØ RET | B-3-32 | Gnd |
| DIN Ø9Ø | B-3-16 | 14-2-16 | DIN Ø9Ø RET | B-3-33 | Gnd |
| DIN Ø8Ø | B-3-17 | 14-2-14 | DIN Ø8Ø RET | B-3-50 | Gnd |
| DIN Ø7Ø | B-3-34 | 14-2-20 | DIN Ø7Ø RET | B-3-35 | Gnd |
| DIN Ø6Ø | B-3-36 | 14-2-18 | DIN Ø6Ø RET | B-3-37 | Gnd |
| DIN Ø5Ø | B-3-38 | 14-1-20 | DIN Ø5Ø RET | B-3-39 | Gnd |
| DIN Ø4Ø | B-3-40 | 14-1-18 | DIN Ø4Ø RET | B-3-41 | Gnd |
| DIN Ø3Ø | B-3-42 | 14-1-22 | DIN Ø3Ø RET | B-3-43 | Gnd |
| DIN Ø2Ø | B-3-44 | 14-1-28 | DIN Ø2Ø RET | B-3-45 | Gnd |
| DIN Ø1Ø | B-3-46 | 14-1-26 | DIN Ø1Ø RET | B-3-47 | Gnd |
| Gnd | B-3-48 | Gnd | Gnd | B-3-49 | Gnd |

DAU BACKPLANE CONNECTOR PIN MAP (BACK-CONN - PIN)
INTERCONNECTION TO INTERDATA 7/32 ULI

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 37 of 38)

CONNECTOR (2) DD - 50S

| FUNC | PIN | FUNC | PIN |
|---|---|---|---|
| DIN ØØØ | T-2-1 | DOT 11Ø | T-2-14 |
| SCLRO | T-2-2 | DOT 1ØØ | B-2-15 |
| SATNO | T-2-3 | DOT Ø9Ø | T-2-16 |
| DRGO | T-2-4 | DOT Ø8Ø | T-2-17 |
| DAGO | T-2-5 | DOT Ø7Ø | T-2-34 |
| COT Ø7Ø | T-2-6 | DOT Ø6Ø | T-2-36 |
| COT Ø6Ø | T-2-7 | DOT Ø5Ø | T-2-38 |
| COT Ø5Ø | T-2-8 | DOT Ø4Ø | T-2-40 |
| COT Ø4Ø | T-2-9 | DOT Ø3Ø | T-2-42 |
| DOT 15Ø | T-2-10 | DOT Ø2Ø | T-2-44 |
| DOT 14Ø | T-2-11 | DOT Ø1Ø | T-2-46 |
| DOT 13Ø | T-2-12 | DOT ØØØ | T-2-48 |
| DOT 12Ø | T-2-13 | Ground | T-2-18/25/50 |

DAU TEST PANEL CONNECTOR PIN MAP (TEST-CONN - PIN)
INTERCONNECTION TO DAU BACK PLANE

TABLE XI - DAU PIN TO PIN WIRING LIST (Sheet 38 of 38)

CONNECTOR (3)

| FUNC | PIN | FUNC | PIN |
|---|---|---|---|
| Ground | T-3-1/18/50 | DIN 12Ø | T-3-13 |
| SIN Ø7Ø | T-3-2 | DIN 11Ø | T-3-14 |
| SIN Ø6Ø | T-3-3 | DIN 1ØØ | T-3-15 |
| SIN Ø5Ø | T-3-4 | DIN Ø9Ø | T-3-16 |
| SIN Ø4Ø | T-3-5 | DIN Ø8Ø | T-3-17 |
| SIN Ø3Ø | T-3-6 | DIN Ø7Ø | T-3-34 |
| SIN Ø2Ø | T-3-7 | DIN Ø6Ø | T-3-36 |
| SIN Ø1Ø | T-3-8 | DIN Ø5Ø | T-3-38 |
| SIN ØØØ | T-3-9 | DIN Ø4Ø | T-3-40 |
| DIN 15Ø | T-3-10 | DIN Ø3Ø | T-3-42 |
| DIN 14Ø | T-3-11 | DIN Ø2Ø | T-3-44 |
| DIN 13Ø | T-3-12 | DIN Ø1Ø | T-3-46 |
| | | DIN ØØØ | T-3-48 |

DAU TEST PANEL CONNECTOR PIN MAP (TEST-CONN - PIN)
INTERCONNECTION TO DAU BACK PLANE

## APPENDIX B

Table XII - DAU Backplane Coaxial Connections

| Connector | Remarks |
|---|---|
| J 1 - 1 MHz RET FREQ | These signals are not brought in through back plane SMA fittings but by running cables directly to the high speed ADC boards. |
| J 2 - 3Ø MHz SIGNAL | |
| J 3 - 3Ø MHz SIGNAL | |
| J 4 - 3Ø MHz Ø$^{O}$ | |
| J 5 - 3Ø MHz -9Ø$^{O}$ | |
| J 6 - Rockland CH 1 (TO) | With respect to the DAU |
| J 7 - Rockland CH 1 (FROM) | |
| J 8 - Rockland CH 2 (TO) | |
| J 9 - Rockland CH 2 (FROM) | |
| J 1Ø - HP 122Ø Scope CH 1 | |
| J 11 - HP 122Ø Scope CH 2 | |

BACKPLANE SMA COAXIAL CONNECTORS

## APPENDIX C

### Table XIII - AP-120B Specifications

FLOATING POINT SYSTEMS AP-120B Array Processor

The AP-120B installed in the Satellite Communications Laboratory includes the following configuration:

| | |
|---|---|
| 768 | words of bipolar RAM program source memory<br>Each word is 64 bits |
| 1024 | words of bipolar RAM table memory<br>Each word is 38 bits |
| 16K | words of MOS RAM main data memory<br>Each word is 38 bits |
| APAL | cross assembler program |
| APEX | executive program |
| APLINK | linking loader program |
| APSIM | simulator program |
| APDEBUG | debugging program |
| APTEST | diagnostic and test program |
| MATH | Library |
| IOP-16 | 16 bit I/O port |

## APPENDIX C

Table XIV - SM-1Ø1 Specifications

SM-1Ø1 Frequency Synthesizer Module made by SYNTEST Corporation.

This is a four and one-half digit modular synthesizer used to provide programmable sample rate for the Data Acquisition Unit.

Ø.1 Hz to 16 MHz in 8 ranges

TTL compatible into 5Ø ohm load

Frequency digitally selectable by BCD TTL lines

Spurious outputs 6Ø db below full output

Setting time 1Ø milliseconds to 1Ø%

Rise time to square wave 8 nanoseconds

Fall time to square wave 8 nanoseconds

## APPENDIX C

Table XV - DATEL SHM and ADC Module Specifications
(Page 1 of 2)

DATEL sample-and-hold modules and analog-to-digital converter modules used in the Data Acquisition Unit.

S/H modules:

| | | |
|---|---|---|
| SHM-5 | Input voltage range | ±1Ø volts |
| | Over voltage range | ±15 volts |
| | Input impedance | 1 M ohm |
| | Gain | -1 |
| | Acquisition time to .1% | 2ØØ nsec |
| | Acquisition time to .Ø1% | 35Ø nsec |
| | Bandwidth tracking | 5 MHz |
| SHM-UH | Input voltage range | ±5 volts |
| | Input impedance | 1ØØ M ohm |
| | Gain | +1 |
| | Acquisition time | 35 nsec |
| | Settled Output | 5Ø nsec |
| | Maximum sample rates | 1Ø MHz |

A/D converter modules:

| | | |
|---|---|---|
| ADC-EH12B3 | Input voltage range | ±5 volts |
| | Input impedance | 1.15 K ohm |
| | Input overvoltage | ±2Ø volts |
| | Parallel output | 12 bits |
| | Serial output | |

## APPENDIX C

Table XV - DATEL SHM and ADC Module Specifications
(Page 2 of 2)

| | | |
|---|---|---|
| | Two's complement, positive true | |
| | Conversion time | 2 nsec max |
| | Start convert | 100 nsec min |
| ADC-VH9B2 | Input voltage | ±1.28 volts |
| | Input overvoltage | ±5 volts |
| | Input impedance | 100 ohms |
| | Parallel output | 8 bit |
| | Offset binary, reverse coding | |
| | Conversion time | 200 nsec |
| | Start convert | 40 nsec |

# APPENDIX D

Table XVI - DAU Signal Reference Chart
(Page 1 of 2)

| Signal Name | Purpose | Reference |
|---|---|---|
| ADC-HI/LO | A/D convert, Mode I control | Table II |
| ADC2-HI/LO | A/D convert, prestart control | Table II |
| ADC3-HI/LO | A/D convert enable | Table II |
| Ain | Enable AP-12ØB output data bus | Figure 32 |
| ASEL/BSEL | Input Selector code select | Table IV |
| BUSYØ, SIN Ø4Ø | DAU busy status | Table VII |
| CS/$\overline{CS}$ | Chip select for buffer memory | Table IV |
| DAGØ(Ø-5) | Control register loading signals | Table VII |
| DAGØB1(Ø)DAGØB2(Ø) | 7/32 WR clocking signals | Table IV, VI |
| DAGØ/DRGØ | 7/32 data transfer signals | Table IV, VI |
| DELAY TIMER | Extra delay for DMA to 7/32 | Figure 25 |
| DRGØB1(Ø)DRGØB2(Ø) | 7/32 RD clocking signals | Table VI |
| $\overline{E}$ ADD | Enable Address register | Table VII |
| EOC HI Chnl/CHn2 | End-of-convert high spd ADC's | Table I, VI |
| EOC LO Chnl/Chn2 | End-of-convert low spd ADC's | Table I, VI |

## APPENDIX D

Table XVI - DAU Signal Reference Chart
(Page 2 of 2)

| Signal Name | Purpose | Reference |
|---|---|---|
| EOCM | End-of-convert-master coincidence of EOC's | Table VI |
| EOM, SIN Ø6Ø | End-of-Medium status | Table VI |
| $\overline{E}$ WC | Enable Word Count Register | Table VII |
| OVØ, SIN Ø5Ø | DAU overrun status | Table VII |
| PWROK | Power OK, all supplies on | Table I |
| Sample Comm HI/LO | Start taking sample | Table I |
| SATNO | DAU to 7/32 interupt | Table VII |
| SEL(TOGGLE F/F) | Output both channels of data in Output Selector | Table IV, VI |
| SYNCBØ | Slave-sync B, end of cycle | Table IV, VI |
| SSYNCB1(Ø) | Delayed SSYNCBØ | Table VI |
| SSYNCB2(Ø) | Delayed SSYNCB1(Ø) | Table VII |
| Start Convert HI/LO | Start A/D conversion | Table I |
| SYNTEST/SYNTEST2 | Sample rate clock | Table II |
| WC-LO, SIN Ø7Ø | Word Count register = zero status | Figure 35 |
| $\overline{WE}$ | Write enable for buffer memory | Table IV, VI |
| 1MHZ | ADC Prestart clock source | Table VII |
| 7/32 RD | Data transfer from DAU to 7/32 | Table VII |
| 7/32 WR | Data transfer from 7/32 to DAU | Table VII |

## APPENDIX E

## DUAL CHANNEL A/D CONVERSION THEORY

The Data Acquisition Unit uses dual channel A/D conversion to produce a wider bandwidth frequency spectrum for a given sample rate and to more efficiently use the FFT algorithm. To understand the mathmatics of dual channel conversion, the following derivation is given:

Given an ideal sinusoidal input as shown in Figure 46(a), where;

input = $\cos(\omega_o+\Delta)t$

L.O. for real channel - $2 \cos \omega_o t$

L.O. for imaginary channel - $2 \sin \omega_o t$

and considering that possible apparent image components which are part of the input signal are;

$\alpha \cos(\omega_o-\Delta)t$

$\beta \sin(\omega_o-\Delta)t$

Taking this ideal case and using appropriate trig identities, Table 46(a), shows the real and imaginary output for each input.

Then the actual case, Figure 46(b), can be considered taking into account possible phase and gain errors where:

input = $\cos(\omega_o+\Delta)t$

L.O. for real channel = $(1+\varepsilon/2)\cos(\omega_o t+\phi/2)$

L.O. for imaginary channel = $(1=\varepsilon/2)\cos(\omega_o t-\phi/2)$

which results in:

$$R' = (1+\varepsilon/2)\cos(\Delta t-\phi/2)$$

$$= (1+\varepsilon/2)(\cos\Delta t\cos\phi/2+\sin\Delta t\sin\phi/2)$$

$$I' = -(1-\varepsilon/2)\sin(\Delta t+\phi/2)$$

$$= -(1-\varepsilon/2)(\sin\Delta t\cos\phi/2+\cos\Delta t\sin\phi/2)$$

for small phase errors

$$\cos\phi/2 \approx 1 \quad \text{and} \quad \sin\phi/2 \approx \phi/2$$

using these assumptions and ignoring second order terms;

$$R' \approx \cos\Delta t + \phi/2\sin\Delta t + \varepsilon/2\cos\Delta t$$

$$I' \approx \underbrace{-\sin\Delta t}_{\substack{\text{actual}\\ \text{signal}\\ \text{out}}} - \underbrace{\phi/2\cos\Delta t}_{\text{term w}} + \underbrace{\varepsilon/2\sin\Delta t}_{\text{term 3}}$$

comparing terms 2 and 3 with those terms in Table 46(a), shows that term 2 can be thought of as the result of an apparent image component ($\beta = -\phi/2$) of;

$$-\phi/2\sin(\omega_o-\Delta)t$$

term 3 can be thought of as the result of apparent image component ($\alpha=\varepsilon/2$) of;

$$\varepsilon/2\cos(\omega_o-\Delta)t$$

These two terms appear to arise from an input image, Figure 46(c), with amplitude;

$$1/2\sqrt{\varepsilon^2+\phi^2}$$

From this the image power to actual power can be compared;

$$\frac{\text{Image power}}{\text{Actual power}} = (\varepsilon/2)^2 + (\phi/2)^2$$

as an example consider;

$$\varepsilon/2 = 2^{o}$$

$$\varepsilon/2 = 10^{-2}$$

then image power to actual power = ;

$$10 \log_{10} \left(10^{-4}+\left(\frac{2\pi}{180}\right)^{2}\right)$$

$$= 10 \log_{10}(10^{-4}+1.22\text{x}10^{-3})$$

$$= -28.8\text{dB}$$

Thus the phase error and gain errors are additive.

After down conversion in the DAU, the baseband signals are amplified and filtered before being A/O converted. This additional signal manipulation causes additional frequency dependent phase shift that must be considered.

$$\theta_1(\omega)|\omega=\Delta=\theta_1 \text{ for real channel}$$

$$\theta_2(\omega)|\omega=\Delta=\theta_2 \text{ for imaginary channel}$$

then including this phase shift in the R' and I' signals gives:

$$R' \approx \cos(\Delta t+\theta_1) + \phi/2\sin(\Delta t-\theta_1) + \varepsilon/2\cos(\Delta t-\theta_1)$$

$$I' \approx \sin(\Delta t+\theta_2) - \phi/2\cos(\Delta t-\theta_2) + \varepsilon/2\sin(\Delta t-\theta_2)$$

ignoring second order terms and assuming for small angles

$$\cos\theta \approx 1 \quad \text{and} \quad \sin\theta \approx \theta$$

$$R' \approx \cos\Delta t + \theta_1\sin\Delta t + \phi/2\sin\Delta t + \varepsilon/2\cos\Delta t$$

$$I' \approx \sin\Delta t + \theta_2\cos\Delta t - \phi/2\cos\Delta t + \varepsilon/2\sin\Delta t$$

$$\text{let } \theta_1 = \theta_0 + \gamma$$

$$\theta_2 = \theta_0 - \gamma$$

then

$$(\theta_0 + \gamma)\sin\Delta t \approx \theta_0 \sin\Delta t + \gamma\sin\Delta t$$

$$(\theta_0 + \gamma)\cos\Delta t \approx \theta_0 \cos\Delta t - \gamma\cos\Delta t$$

and

$$R' \approx (1+\theta_0)\cos\Delta t + (\gamma+\theta/2)\sin\Delta t + \varepsilon/2\cos\Delta t$$

$$I' \approx \underbrace{(1+\theta_0)\sin\Delta t}_{\substack{\text{actual}\\ \text{signal}\\ \text{out}}} - \underbrace{(\gamma+\theta/2)\cos\Delta t}_{\text{term 2}} + \underbrace{\varepsilon/2\sin\Delta t}_{\text{term 3}}$$

comparing terms to Figure 46(a), the ratio of image to signal power is;

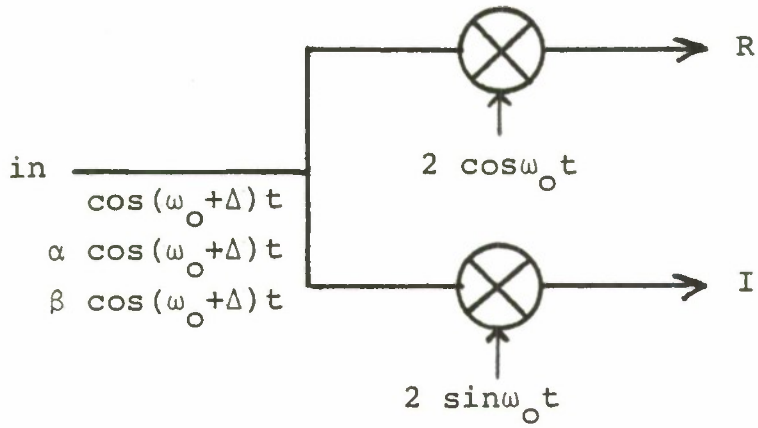
$$\frac{\text{Image power}}{\text{Actual power}} = (\gamma+\phi/2)^2 + (\varepsilon/2)^2 \qquad (1)$$

where $\gamma$ = baseband phase shift

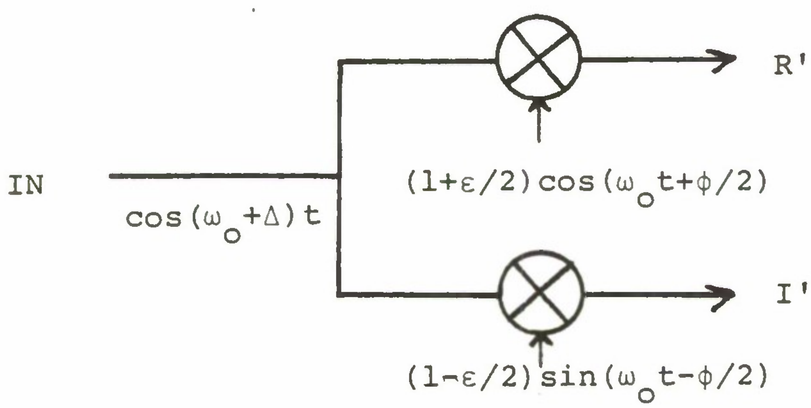
$\phi/2$ = L.O. phase shift

$\varepsilon/2$ = gain error

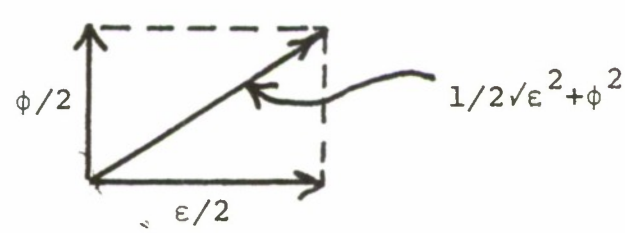
The image power to actual power ratio for different values of gain or phase error has been shown as examples in Table 46(b) and (c). It is important to remember that $\gamma$ is a function of frequency that cannot be adjusted. The phase shift $\phi$ can be adjusted to a minimum and gain error $\varepsilon$ can be adjusted to a minimum. Therefore, the largest contribution to phase error and hence image frequency will be $\gamma$, the baseband phase shift.




a) ideal signals




b) actual signals




c) image amplitude

Figure 46 - Dual Channel ADC Theory

TABLE XVII - DUAL CHANNEL ADC THEORY

| IN | OUT R | OUT I |
|---|---|---|
| $\cos(\omega_o+\Delta)t$ | $\cos\Delta t$ | $-\sin\Delta t$ |
| $\alpha\ \cos(\omega_o-\Delta)t$ | $\alpha\cos\Delta t$ | $\alpha\sin\Delta t$ |
| $\beta\ \cos(\omega_o-\Delta)t$ | $-\beta\sin\Delta t$ | $\beta\sin\Delta t$ |

(a) Ideal signal components

| $\varepsilon$ | % voltage error | image down |
|---|---|---|
| $10^{-2}$ | 1% | -46dB |
| $10^{-1}$ | 10% | -26dB |

(b) Image component with $(\gamma+\phi/2)^2=0$

| $(\gamma+\phi/2)$ | image down |
|---|---|
| $1^o$ | -35.2dB |
| $2^o$ | -29.1dB |
| $5^o$ | -21.1dB |

(c) Image component with $(\varepsilon/2)^2=0$

# GLOSSARY OF TERMS

| | |
|---|---|
| SATCOM | Satellite Communications |
| NAVPGSCOL | Naval Postgraduate School |
| FLTSAT | Fleet Satellite |
| GAPFILLER | An Orbiting Satellite |
| NAVELEX | Naval Electronics Command |
| FSM | Fleet Satellite Monitor |

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